Test Station for the CARIOCA FE-chip of the LHCb Muon Detector

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Abstract

This document describes the hardware and the software of a Front-End Electronics Test Station developed to test and characterize the Front-End ASIC for the LHCb Muon chambers. This ASIC, an 8-channel amplifier, shaper and discriminator with baseline restoration, processes read-out signals generated by Multi-Wire Proportional and GEM chambers located in a high radiation environment. It is almost entirely analog. In total, an amount of about 25000 chips will be produced in both the engineering and production runs. They will require individual testing, before final assembly on printed circuit boards. The test system we present has the following features: variable and bipolar charge injection, custom read-out, rate and time measuring circuitry, power consumption control, data analysis and statistical tools. The system is controlled by a LabVIEW based program. We present the results of about 3000 tests of ASIC produced in the engineering run.

I. INTRODUCTION

The LHCb Muon Group has developed a CMOS ASIC using a rad-hard IBM 0.25μm process for its read-out system, composed of Multiwire Proportional Chambers (MWPC) and Triple Gas Electron Multiplier (GEM) detectors [1-2]. Each CARIOCA (Cern And RIO Current-mode Amplifier) [3] holds 8 identical channels of current-mode Amplifiers, Shapers and Discriminators with Baseline restoration (ASDB). Two different versions have been implemented: one to process MWPC cathode and anode signals, designed for 5 ns peaking time, 0.5 fC equivalent noise charge for a typical detector capacitance of about 25 pF and a tail cancellation circuit; another one to process GEM detector signals, without ion tail cancellation circuit, and reduced minimum detectable charge from 3 fC to 2 fC delta pulse equivalent.

The Front-End Electronics Test Station (FEET) has been devised to accomplish bipolar tests and to measure characteristics of both CARIOCA versions. All tests should be carried out before chips are soldered to front-end boards (FEB), in order to minimize potential over-costs related to loss of time and rework activities if a significant proportion of boards is found to be defective. Each FEB will have two CARIOCA and an additional ASIC, name DIALOG (Diagnostics, time Adjustment and LOGics), designed to handle 16 CARIOCA outputs.

Initially designed to test FE-boards [4], the FEET system has been adapted to test single CARIOCA. In the development phase, procedures have been established and some parameters had to be investigated with greater accuracy. Several algorithms have been implemented to achieve a systematic test procedure for the detector read-out apparatus. The parameters under test are: power consumption, threshold offset, sensitivity, time-walk and pulse width. Dead or open channels are also identified (connectivity tests).

The system is being used to characterize the chips produced in the last engineering run before final production. We present results for both CARIOCA and CARIOCA-GEM versions.

II. FEET DESCRIPTION

The main building blocks of FEET are a charge injector, a read-out and counting device, a Time to Digital Converter (TDC) custom circuit, a National Instruments data acquisition (NI-DAQ) PCI board and an integrated LabVIEW program. The Injection Board (IB) contains 8 channels and its circuitry permits a fine tuning of injected charge (in the range of few fC) and of ASD threshold values, since CARIOCA has 8 individual threshold inputs. It can also mask out any chosen group of channels, control the injection rate and finally inject either positive or negative charge as required. A Counting Board receives differential signals from the ASIC under test and processes data by means of 8 counters (all synchronized to IB signals); it transfers data to a local computer via the NI-DAQ board and its functionalities are based mainly on a Xilinx FPGA implementation. The custom TDC module receives signals generated by CARIOCA and by the injection system, and measures time-walk and pulse width.

The hardware is arranged in different modules, which are introduced in the next sub-sections.

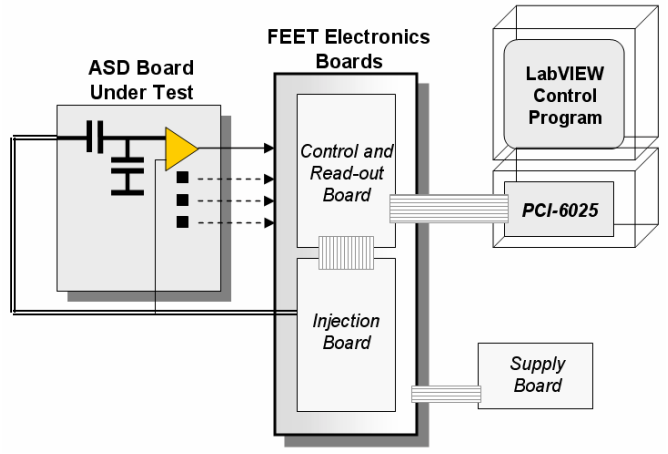

Figure 1: FEET System block diagram.

A. Data-Flow

The injection board contains 8 lines and its circuit permits to control threshold and injection charge values, enable or disable such lines and adjust injection rate. Control and read-out board manages injection circuit parameters, read-out the front-end electronics output signals and process data by means of multiplexers and counters. It contains also the necessary logic to communicate with PC via NI-DAQ. More than allowing FEET-PC interface, NI-DAQ circuitry distributes synchronous clocks and provides referential signals for threshold and charge injection circuits.

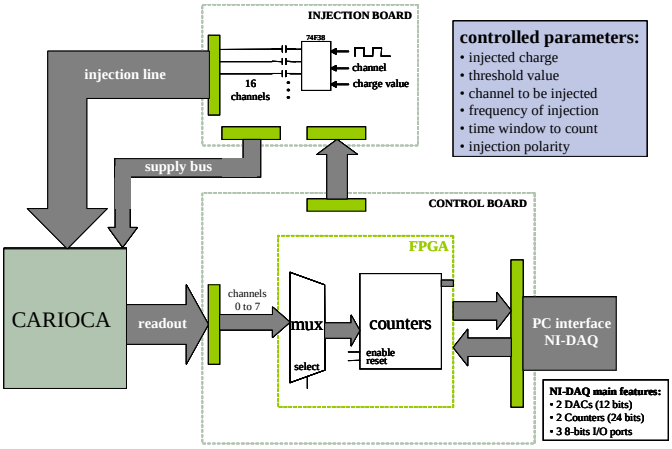

Figure 2: FEET data-flow.

B. Control and Read-out Board

This board has been developed to control the injection structure and to read the front-end LVDS-based output. A data-transfer custom protocol has been implemented as well. Its logics are based mainly in a FPGA VHDL implementation (Fig. 3) and a few external components. Latches have been used to enable and disable injection lines (see Fig. 4 'channel select') and a differential line receiver for the FE signals readout.

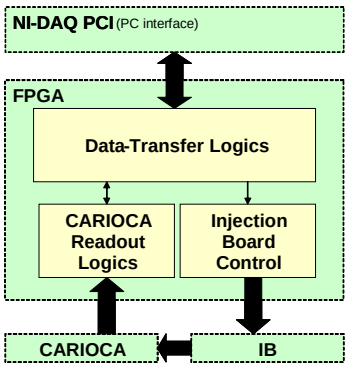

Figure 3: FPGA logics diagram.

The main components are presented below:

- FPGA SRAM Xilinx 4010E
- EEPROM Xilinx 18V256
- DS90C032TM (differential line receiver)
- 74LS374 (8-bits latch)

C. Injection Board

This board is based on a component (74F38) which offers four independent gates which implement the NAND logic function, each one with an open-collector output. Such a component allows adjustment of injected charge, control of output enable and rise time transition of about 3 ns. 8 injection lines have been implemented for CARIOCA tests.

Fig. 4 shows how injection lines are controlled and how charge is injected. '*channel select*' is controlled by FPGA via external latches while 'strobe' is generated by NI-DAQ circuitry. '*strobe*' generation is synchronized with a second clock with a phase difference of 90° or 270° depending on the injected charge polarity. Such a clock controls the FPGA implemented counters enable.

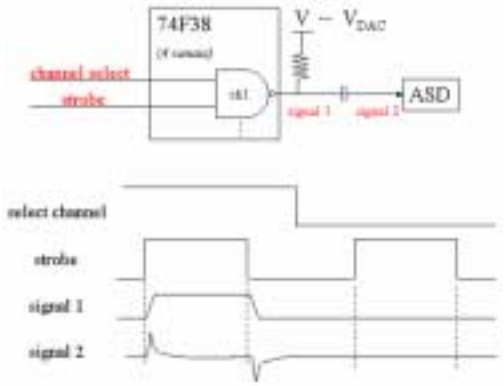

Figure 4: Injection scheme.

D. TDC Board:

The TDC module consists of two circuits: the TDC circuit, based on the commercial TDC IC F1 of ACAM, with eight stop channels and one common start channel, and an interface board which transmits data to a PC via the parallel port. The integrated circuit F1 converts LVDS signals with a minimum

resolution of 120 ps. The signal injected to CARIOCA is splitted to compose the start signal of the TDC. The 8 LVDS CARIOCA outputs give the stop signals. The time difference between the start and the first transition of the stop signals define the time walk. The time difference between the two LVDS signal transitions is defined as time width.

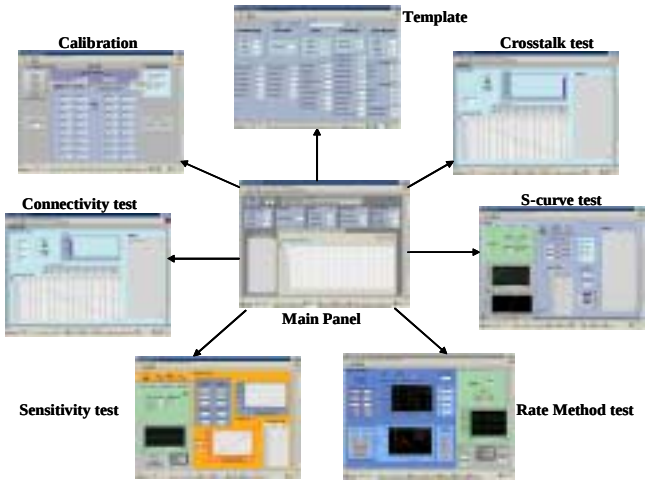

Figure 5: Software diagram.

E. LabVIEW based program

The software has been developed to remotely control all the system and to perform automatic test procedures. It allows also an easy-to-use framework for adjustment of test parameters (more than 40 parameters), offering an exclusive window interface for each test procedure (Fig. 5). An auto-calibration procedure has also been foreseen to perform calibration of FEET injection lines once a well-known FE chip is given.

At the end of every test a database is created with results and test crude-data which consents future reconstruction of characterization curves and results.

III. TEST RESULTS

We have tested up to now about 2500 CARIOCA and 500 CARIOCA-GEM. The system has been calibrated to yield an average sensitivity of 12 mV/fC, for a detector capacitance of 150 pF. About 9% of the chips tested presented dead or open channels. Power consumption has been very stable. The ASIC is supplied with 2.5 V and draws an average current of 132 mA. A Gaussian fit yields a sigma of (1.89±0.03) mA, as can be seen in Fig. 6.

Figures 7 and 8 show the 8-channel average of the sensitivity, in mV/fC, and noise, in fC. Gaussian fits have sigma variances of 0.5 mV/fC and 0.07 fC, respectively. The minus sign in the sensitivity is due to the injection of negative polarity signals.

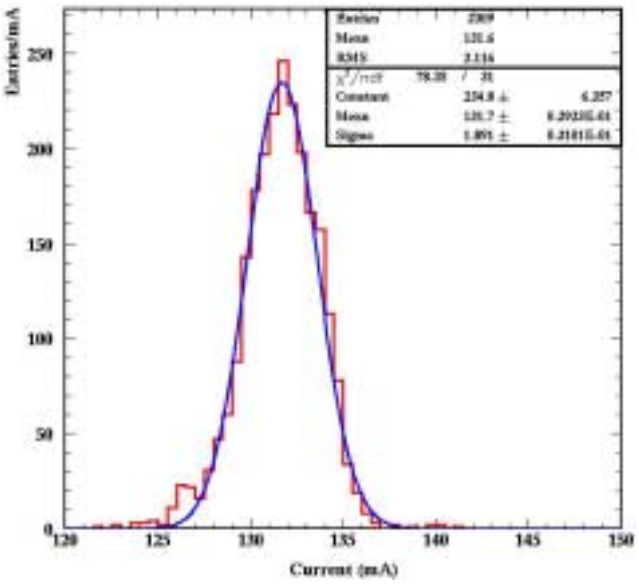

Figure 6: Current distribution of CARIOCA chips.

Figures 9 and 10 show the time width and threshold offset mean values as a function of the chip channel. Error bars correspond to RMS values of the distributions. For the threshold offset, a typical RMS value is of the order of 40 mV (~5 % of the mean value). For time width, the RMS is around 500 ps (~2% of the mean value). The time width is measured at a threshold of 1000 mV and an input charge of 100 fC.

The CARIOCA-GEM characterization presents similar behaviour. The average sensitivity was measured ar 18.5 mV/fC, about 1.5 times the average CARIOCA sensitivity, as expected. The same ratio is observed between the CARIOCA-GEM and CARIOCA time widths.

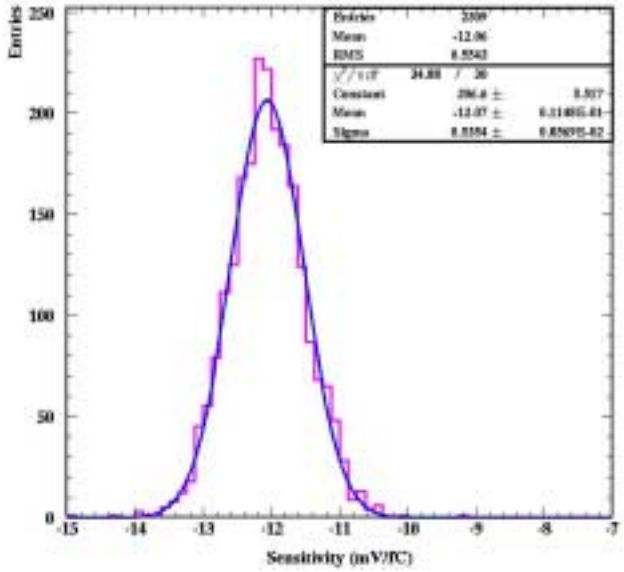

Figure 7: Sensitivity distribution of CARIOCA chips.

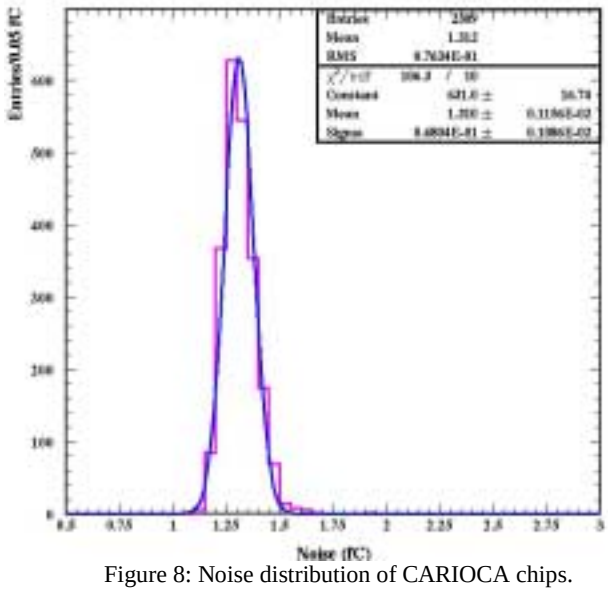

Figure 8: Noise distribution of CARIOCA chips.

The parameter which can mostly reject chips is the sensitivity. By requiring that all channels have both sensitivity and offset within ± 10% of the chip average, chips are rejected with a rate of 25%, with respect to the number of chips which passed connectivity cuts. Figure 11 shows the evolution of the failure rate as a function of offset and sensitivity uniformity cuts. If the requirement is released to sensitivity uniformity within 20%, then only 5% of the chips are rejected.

IV. CONCLUSION

A test station has been developed to characterize the CARIOCA front-end chips for the LHCb Muon chambers. About 3500 chips have already been tested. The failure rate due to dead or open channels is about 9%. In addition, about 25% of the CARIOCA present either sensitivity of offset variation in at least one of the 8 channels above ± 10% of the chip average. For CARIOCA-GEM, the failures due to sensitivity and offset are at the level of 13%.

Using this test bench, a characterization rate of 100 chips per day could be achieved.

V. AKNOWLEDGEMENTS

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VI. REFERENCES

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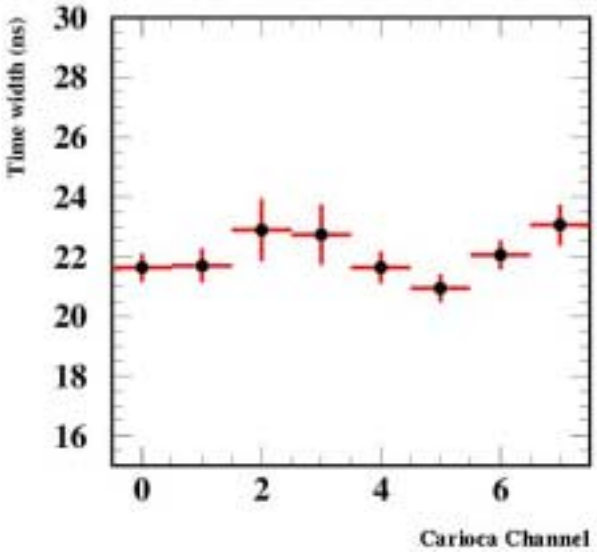

Figure 9: Time width of output signal as a function of chip channel.

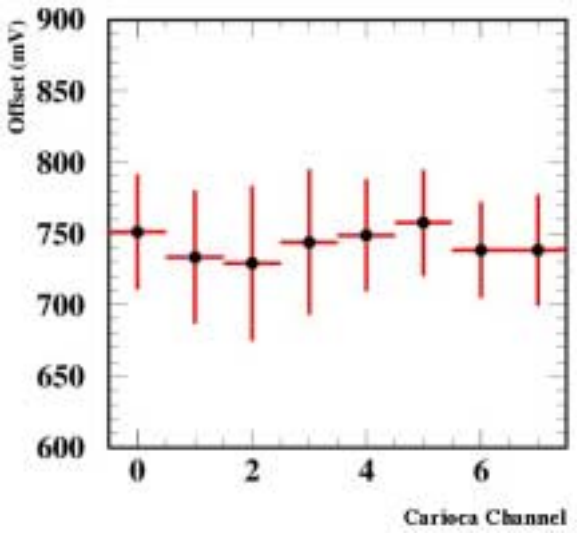

Figure 10: Mean threshold offset as a function of IC channel.

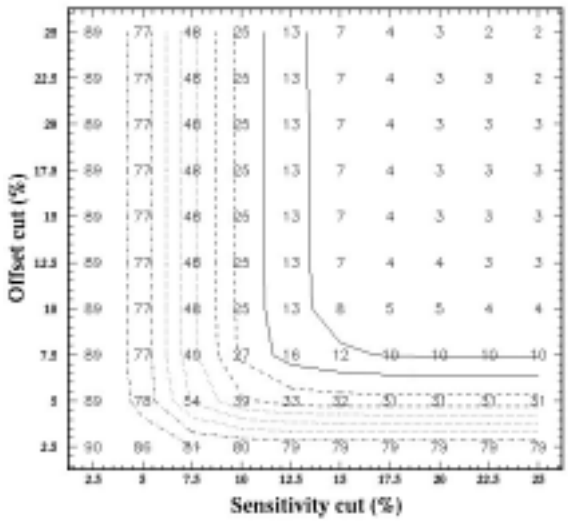

Figure 11 – CARIOCA rejection rate as a function of the uniformity cuts on threshold offset (vertical axis) and sensitivity (horizontal axis). Cuts are defined as a fraction of the 8-channel chip average.