An Image Acquisition System Based on State Machine and Sampling ADCs

Herman P. Lima, Jr., Ademarlaudo F. Barbosa, Germano P. Guedes, and Luciano M. de Andrade Filho

***Abstract*—The present work reports on the development of a digital system for image acquisition which is able to process two electric signals of amplitude varying between 0 and 10 V. The system correlates both signals in a two-dimensional (2-D) histogram. X and Y coordinates for every event are obtained from the amplitudes of two coincident signals. The hardware consists of two analog-to-digital converters (ADCs), two complex programmable logic devices (CPLDs), and one 2 MB static random access memory (SRAM), implemented in a card that is plugged into personal computers. The data acquisition rate may be as high as 1.0×10^6 events per second, and does not depend on the PC processor. The software code has been written in the Delphi environment using Assembly routines for the I/O bus operations. Image sizes may be chosen from 128×128 up to 1024×1024 pixels and may be viewed in color scale, with two or three-dimensional graphics. Images are shown to illustrate the applicability to two-dimensional position sensitive X-ray detectors.**

***Index Terms*—Analog-to-digital converter (ADC), image acquisition, programmable logic device, state machine, X-ray detectors.**

I. Introduction

PARTICLE detectors that use gas as the absorbing medium and wires as charge collection electrodes [1] are widely used in several applications, covering the range from simple counters up to large area two-dimensional (2-D) position sensitive detectors. These applications require the use of electronic modules [preamplifiers, amplifiers, discriminators, external delay, and time-to-amplitude converters (TACs)] and a data acquisition system to acquire and visualize the data. In the case of one-dimensional position sensitive particle detectors [2], the position coordinate of a photon may be represented by a proportional voltage amplitude in the TAC output. Analog-to-digital conversion of the TAC output therefore provides the photon position information. The two-dimensional data acquisition system (TDAS) presented here performs the analog-to-digital conversion of two TAC outputs, corresponding to the X and Y coordinates of the event. The digital X and Y words are grouped to define one address on the memory address bus. A histogramming circuit accumulates events in specific memory positions over a period of time, constructing an image. The present work proposes a new scheme for the TDAS which is based on the use of a logic state machine, implemented in programmable logic devices, instead of a microprocessor to control and process the digitized data. Fast ADCs in single-shot mode are used to digitize the input signals. Combining fast ADC conversion speed with digital data processing based on a state machine, we achieve low dead time for this particular position readout technique.

Manuscript received November 25, 2001; revised March 15, 2002 and April 1, 2002. This work was supported by CNPq (Brazilian national research funding agency) and FAPERJ (Rio de Janeiro research funding agency). The present work has been developed in the Brazilian Center for Physical Research (CBPF-Brazil).

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Digital Object Identifier 10.1109/TNS.2002.803887

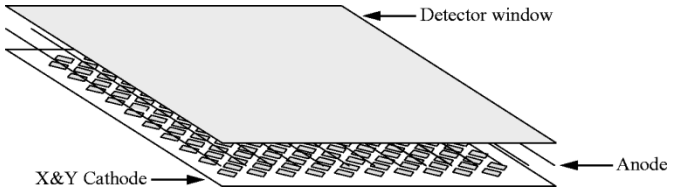

Fig. 1. Scheme for the MWPC with discrete cathode sampling elements.

II. The Position Sensitive Detector

The proposed image acquisition system is intended to be used with an X-ray gas position sensitive detector (PSD) to acquire two coordinates of the position of detected photons. The detector uses a single electrode, called the X&Y cathode, to sense the electric charge induced by ionization avalanches generated by the absorption of X-ray photons in a multiwire proportional counter (MWPC) [3]. Fig. 1 shows the scheme of a MWPC where one of the conducting planes is the detector window, and the other is subdivided in discrete sampling elements, composing the X&Y cathode. The X&Y cathode is a compact multilayer printed circuit board which does not involve wires. Two-dimensional localization of photons is achieved by associating one delay line to each coordinate. The discrete cells of each delay line are properly connected by conducting strips to the corresponding sampling pads so that the propagation time of electric pulses can be related to the avalanche position [4]. The data and results presented here refer to a 2-D detector with an 8 cm $\times$ 8 cm beryllium window, filled with an Argon-Methane gas mixture at 0.1 atm above normal pressure. The anode is constructed with 10 μm gold coated tungsten wires, at a 1 mm pitch. The gap between anode and X&Y cathode planes is 4 mm.

III. Readout Electronics

Signals coming from the delay lines feature a very small amplitude (typically < 1 mV). A preamplifier is therefore required as the first stage in the readout chain. After preamplification, signals are sent to the amplifier and discriminator modules in order to define precise timing criteria. The most basic of the timing techniques is based on the use of leading edge discriminators. This technique uses a circuit which compares the signal

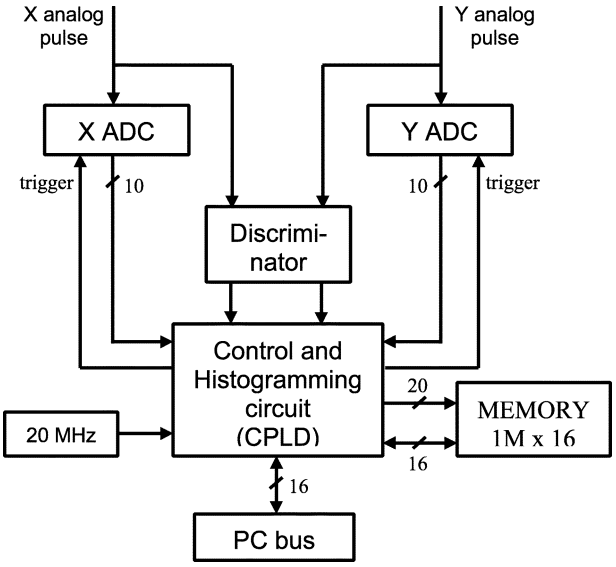

Fig. 2. Simplified block diagram of the digital circuit for image acquisition.

amplitude to a pre-set value above the electronic noise. Whenever a photon is detected, the amplitude at the circuit input is higher than the pre-set value and a fast logic pulse is generated, indicating that a valid event has occurred. However, this timing technique incorporates some error depending on the input signal amplitude, since the preset comparison voltage is fixed while the signal amplitude varies. This error is compensated for by use of constant fraction discriminators, in which the timing signal is emitted when the input signal reaches a given fraction of its maximum amplitude.

The information concerning the $X\&Y$ coordinates of an event is represented by the interval between the electric signals coming from both ends of each delay line. This interval is measured by the TACs. Each TAC converts the time delay between two logic pulses to a proportional amplitude pulse. Thus, at the last analog stage of the readout chain, two analog pulses corresponding to the $X\&Y$ coordinates of each photon absorbed at the detector are available for digitization.

In our current experimental setup we use homemade preamplifiers [5], Philips Scientific 715 constant fraction discriminators, and Ortec 566 TACs.

IV. Two-Dimensional (2-D) Data Acquisition Circuit

The complete detection system includes the detector itself, the readout electronics, the digital circuitry for two-dimensional 2-D data acquisition and a software interface. A block diagram of the TDAS is shown in Fig. 2 and briefly described later.

A. Analog-to-Digital Conversion (ADC)

We have selected the AD1671KP converter manufactured by Analog Devices to digitize the analog input pulses. It is a monolithic 12 bit, 1.25 MSPS ADC with an on-board, high performance sample-and-hold amplifier and voltage reference. The AD1671 uses a subranging flash conversion technique (also called multiple-step parallel) [6], implemented in a high speed bipolar/CMOS process. A single pulse is used to initiate the conversion process, which is finished about 800 ns later, indicated by a single output pulse. Aside from fast conversion, the AD1671 presents another important feature for our design: it is not a free-running, pipelined ADC, which simplifies the design since in our application the conversions are event-triggered, and the events occur randomly in time. In order to improve the image quality we use only the ten most significant ADC bits, resulting in a reduced differential nonlinearity of ± 0.5 LSB, instead of ± 2.0 LSB, specified for the converter. This approach was tested in a design of a multichannel-analyzer and has proved its efficiency [7]. We have also designed a digital right shifter, which acts on the memory address bus and allows one to decrease the image resolution down to 128×128 pixels, increasing the counting rate per pixel and the image update speed on the PC screen.

B. Discriminator

The two analog pulses coming from the TACs are sent to the ADCs and to a leading edge 2-channel discriminator. The discriminator circuit includes fast comparators that perform noise rejection and pre-trigger action. When the analog input pulses exceed an adjusted threshold, digital pulses are generated at the output of the comparators, starting the ADC trigger processes. We use a dual ultrafast TTL comparator, MAX912. It features fast propagation delay (10 ns), low supply current, and a wide common-mode input range, which supply design demands with a bit of signal conditioning.

C. Digital Circuitry

All the control signals and the histogramming process are generated by digital logic implemented in two complex programmable logic devices (Xilinx XC9500 family), which use a 20-MHz clock for timing. Each CPLD presents 7.5 ns pin-to-pin logic delays on all pins, containing 108 macrocells with 2400 usable gates. The following sections describe the main digital modules and their functions.

1) Coincidence Logic: Once a time coincidence occurs between the two analog pulses from the TACs, a trigger pulse is generated by a digital scheme and sent to the ADCs, indicating that a valid event occurred in the detector active window. The digital scheme for coincidence verification receives the outputs of the TDAS discriminator and provides a single trigger pulse to the ADCs if both edges of the input signals occur within a 300-ns window. In addition to the coincidence function, this circuit introduces a delay of 550 ± 50 ns between activation and generation of the trigger pulse. This is done to avoid sampling of the TAC signal in its rising edge region, where the amplitude is not yet stable.

2) Histogramming and Control Circuits: After the analog signals have been digitized, the histogramming process is initiated. In order to deal with this process, a logic state machine was designed, clocked by a 20-MHz signal. The machine uses four clock cycles to perform the reading, incrementing, and writing of data to the memory addresses. A 200-ns interval is therefore enough to complete the state machine action for each event. It operates in continuous mode during data taking, only pausing during a host PC access. During this period, the host takes the address and data buses of the on-board memory, reading their

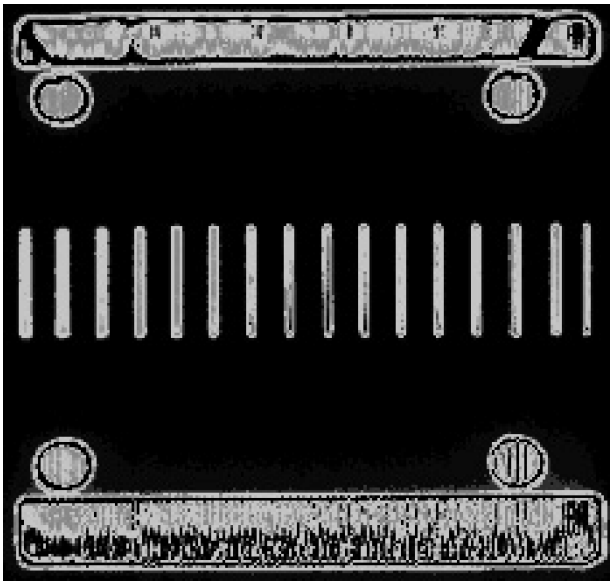

Fig. 3. Image used for linearity and spatial resolution estimation in the X direction.

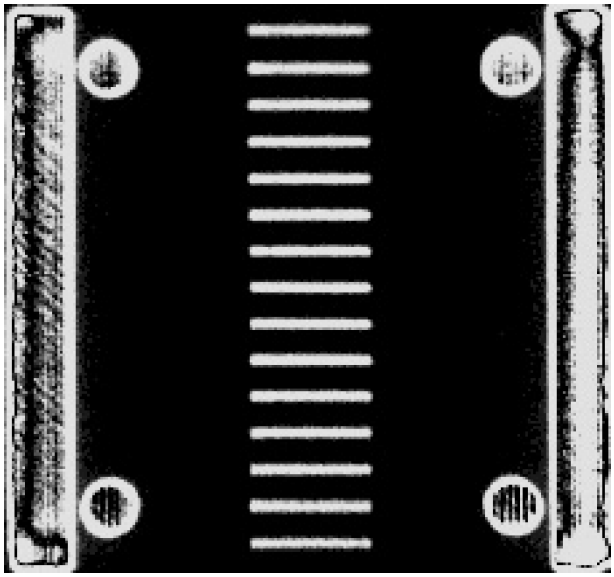

Fig. 4. Image used for linearity and spatial resolution estimation in the Y direction.

contents and resetting them when finished. Finally, an updated image is displayed on the PC screen. The updating process is fast enough to provide almost real-time image acquisition in generally used PCs.

The control circuit functions are: global enable, memory access control (including data/address buses and read/write/enable pins) and ADC data shift. These operations are carried out by the use of I/O instructions and D flip-flops to latch control signals. The global enable signal is used to take the memory control pins to tristate, disabling any data access, and to latch the comparator outputs, disabling any start of conversion. The memory access control is done by multiplexing all memory pins and buses, allowing access by the host PC and by the histogramming circuit. Also inside the CPLD an ADC data shifter is implemented, which is equivalent to a memory address shifter, since each possible ADC data output is treated as a memory address. The shifter circuit allows one to vary the image resolution from 128×128 up to 1024×1024 pixels.

V. Results

In order to evaluate the system performance, concerning the image quality, we execute two main tests. First, we illuminate the detector window with an ^{55}Fe X-ray source through a 2.0 mm thick mask containing regularly spaced slits (5.0 mm pitch). Each slit is 0.3 mm wide. From the resulting images, as shown in Figs. 3 and 4 , we are able to estimate the linearity and spatial resolution of the image acquisition system in both X and Y directions. In the second test, we obtain images of real objects by illuminating the detector with the same source. The results are shown in the following sections.

A. Linearity

For the linearity measurement, we use transverse cuts of the image corresponding to the array of slits illustrated in Figs. 3 and 4. These cuts provide peaks associated with each slit in the mask. By fitting each peak with a Gaussian function, we obtain the central position, in channels, for each peak. Since the distance between the slit centers is constant, the relation between the peak centers and the slit positions should be linear. We assume the maximum deviation from a linear fit as the linearity error of our system. However, the peaks closer to the detector window edge have a bigger error due to parallax effect (finite source to detector distance) and other edge effects (from the delay line and the wire electrode). Neglecting these peaks, the measured linearity error is approximately 0.1% for both the X and Y directions.

B. Spatial Resolution

The central peak in the array of peaks referred to in the previous section is the one with the least parallax error, since the slit in this case is facing the X-ray source. This peak may best be used in an estimation of the spatial resolution. Fig. 5 shows the peak profiles in the X and Y directions, with a Gaussian curve fit to each of them.The full width at half maximum (FWHM) and the spatial resolution (R) are related by

$$R = \sqrt{\text{FWHM}^2 - S^2} \tag{1}$$

where "S" is the detector width effectively illuminated by the x-ray source through the slit. Due to the geometric parameters of the experiment, 'S' is slightly bigger than the slit width. It is derived from elementary geometric considerations and is given by

$$S = \frac{D \times F + k \times d}{D - k} \tag{2}$$

where "D" is the source-to-anode distance, "F" is the slit width, "k" is the slit-to-anode distance and 'd' is the source width (Fig. 6). We find that the spatial resolution is 0.65 mm in the X direction, and 0.92 mm in the Y direction.

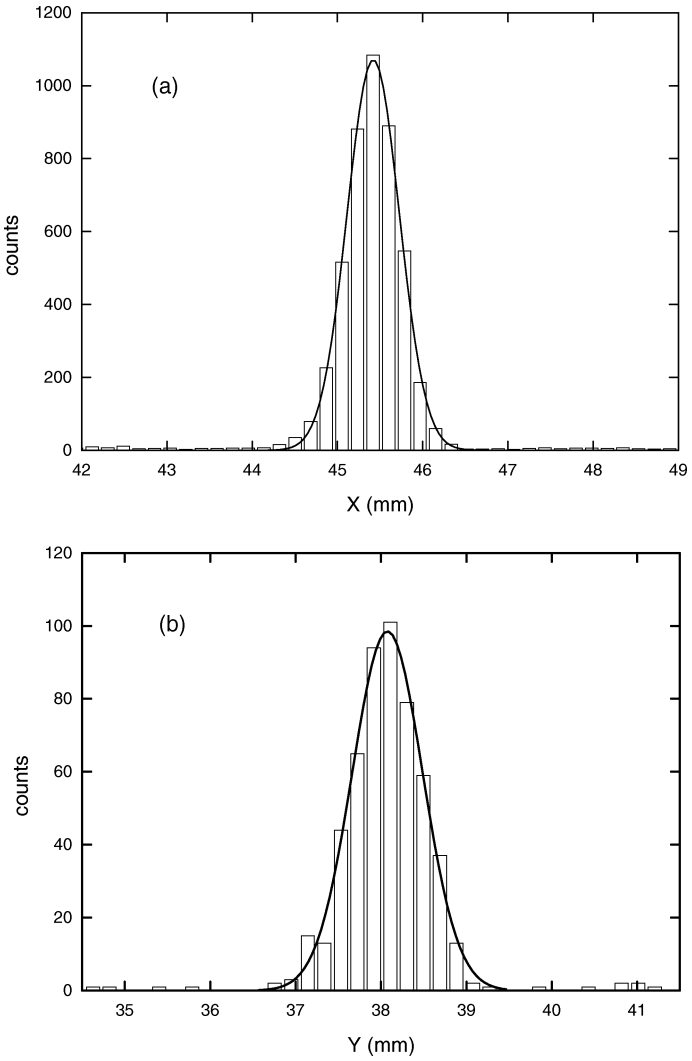

Fig. 5. Peak profile in the (a) X and (b) Y directions.

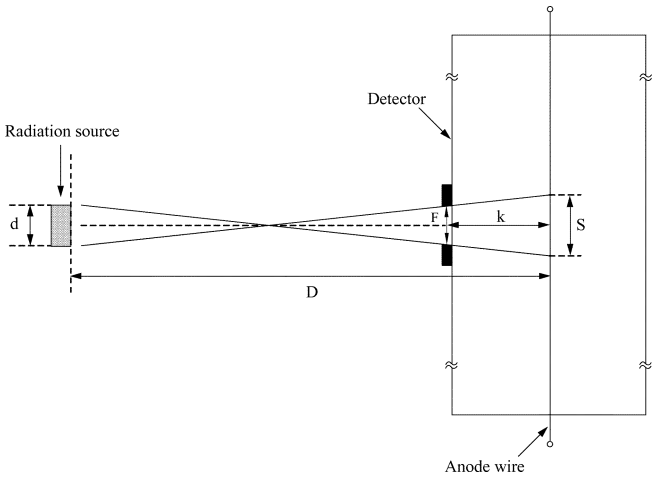

Fig. 6. Geometric parameters referred to in (2).

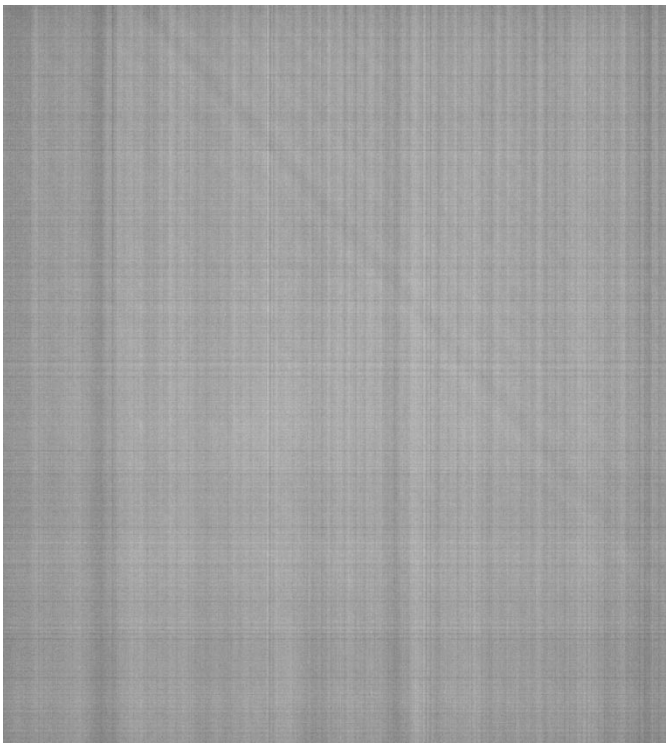

Fig. 7. Response of the detector to illumination by an ^{55}Fe source, with 1024×1024 pixel resolution.

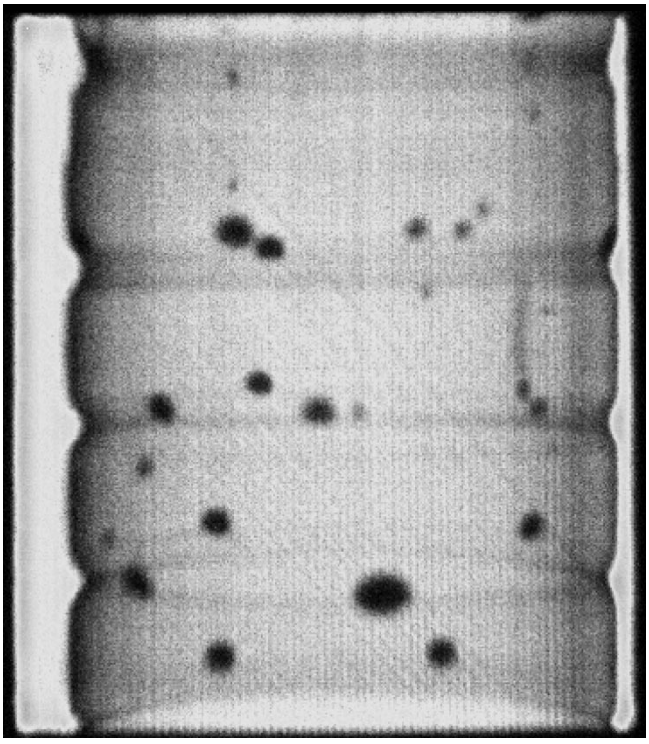

Fig. 8. X-ray image, with 512×512 pixels, of an empty mineral water bottle with some remaining bubbles.

C. Images

Fig. 7 is the image obtained by illuminating the detector with an ^{55}Fe X-ray source placed about 50 cm away from its window for a few hours. For this image, we used 1024×1024 pixel resolution and obtained around 1000 counts per pixel. This test illustrates fairly good image homogeneity. In Fig. 8, a 512×512 pixel image of an empty mineral water bottle is shown. It is seen that the remaining water bubbles are thick enough to completely absorb the radiation, while the plastic bottle material is almost transparent. Some modulation is seen in the images, related to the 1-mm anode wire pitch.

VI. Conclusion

A high-speed image acquisition system with a 2-D position sensitive detector, standard readout electronics and a new digital circuit for data acquisition is presented. The digital circuitry has been implemented in a card for the ISA bus of PCs, since it does not require the outstanding features of the PCI bus. By using 1.25 Msps ADCs and complex programmable logic devices, we achieve a data acquisition rate slightly above 1.0×10^6 events per second. The global counting rate is presently limited by the ADC sampling rate. Images may be visualized with up to 1024×1024 pixel resolution. Linearity tests have been done, resulting in errors lower than 0.1%. The spatial resolution is below 1 mm in both X and Y directions, limited by the detector anode wire pitch.

Acknowledgment

The authors are grateful to P. R. Marinho for his support on setting up the 2-D detector electronics.

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