A Fast Multichannel-Analyzer for Radiation Detection Applications

Herman P. Lima, Jr., Germano P. Guedes, Ademarlaudo F. Barbosa, and Jose M. Seixas

***Abstract*—This work reports on the development of a multichannel analyzer (MCA) circuit for use in radiation detection. The MCA is based on a fast analog-to-digital converter (ADC) plus a digital circuitry programmed on a complex programmable logic device (CPLD). The ADC digitizes the input signals with high accuracy and low nonlinearity while the CPLD performs the histogramming process of the acquired voltage amplitudes. The MCA basic operations are carried on by a logic state machine implemented in the CPLD, triggered by a 20-MHz clock. This approach has allowed us to reduce the circuit dead time to 200 ns. Other performance parameters are related to the used ADC chips. Results are shown that illustrate competitive results as compared to commercially available MCAs.**

***Index Terms*—Discriminator, multichannel analyzer, position-sensitive detector, programmable logic, state machine.**

I. Introduction

MULTICHANNEL analyzers are widely used in different applications requiring counting and amplitude sampling of a varying signal. The most general application in nuclear sciences is possibly ionizing particles spectroscopy, where the particle energy is estimated from the amplitude of the electric signal generated in a detector by an interaction of the particle with the detection medium. In some position-sensitive detectors [1], a voltage amplitude corresponding to the particle spatial coordinates also has to be digitized and histogrammed [2]–[4]. The MCA described here was developed for use in an X-ray detection system where the photon position in one dimension is related to the time interval corresponding to signal propagation through a delay line [5]. In this case, the time interval is converted to a voltage amplitude which is, therefore, associated to the spatial coordinate. Such detection systems include the detector itself, analog processing electronic modules [basically pre-amplifiers, amplifiers, discriminators and time-to-amplitude converters (TACs)], the digital circuitry for data acquisition represented by the MCA, and a software interface for data storage, control, and display. The MCA performs the analog-to-digital conversion of input signals and counts each amplitude on a specific channel, represented by a memory location. Some years ago, the MCAs were manufactured as a separated and independent unit. Lately, they are usually plugged to the I/O bus of personal computers (PCs) [8], and contain an on-board Wilkinson [6] or successive approximation [7] analog-to- digital converter (ADC) and memory chip, featuring 1- to 16- K channels.

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The present work refers to a new MCA scheme based on the use of a programmable logic device instead of the microprocessor typically used in most MCAs. As a matter of fact, the basic digital operations required by an MCA are very simple (namely read, increment, and write data to a memory location) when compared to the possibilities of microprocessors and microcontrollers. On the other hand, any action performed by such devices requires a minimum number of assembly instructions and the associated clock periods. Our approach consists in providing a logic device which only does the digital operations required by the MCA, and arranges that these operations are triggered and completed by hardware. This technique speeds up data acquisition, since it reduces the processing dead time. Fast sampling ADCs are used to digitize the input signal. Combining low-conversion ADC time with a high-speed digital signal processing using CPLDs, we have reached maximum data acquisition rate. The maximum rate is actually limited by the ADC conversion time. Using a relatively slow (20-MHz) clock, we are able to process all the histogramming operations associated to an event (a detected particle, for example) in 200 ns, while the conversion time of high resolution ADCs is typically in the range of 1 μs. In order to improve the MCA performance, ADC selection was mainly focused on low differential nonlinearity (DNL) devices, since linearity has a major impact on the quality of data provided by position-sensitive detectors [9].

II. Circuit Description

An MCA is, in principle, equivalent to many independent pulse height analyzers with their windows arranged contiguously [10]. A typical MCA includes the following main parts: analog circuitry, ADC, memory, and digital circuitry. The analog input signal first passes through linear devices such as comparators, linear gates, or operational amplifiers. ADC and memory are commercially available chips. The MCA scheme here proposed maintains the basic elements described above, but it presents the innovation of using a programmable logic device (CPLD) instead of a microprocessor to control the digital data processing. Fig. 1 is a block diagram of the developed circuit. The input signal is an analog pulse provided by any low output impedance source, for instance the output of a time-to-amplitude converter. It is sent to a discriminator unit, which is in fact a comparator emitting a digital pulse whenever the amplitude at the input is higher than an adjustable threshold. A dual monostable multivibrator is then used to generate the ADC trigger pulse. The pulse width of one of the monostables is trimpot tuned. At the end of this pulse, the trigger pulse is emitted by another monostable, which enables

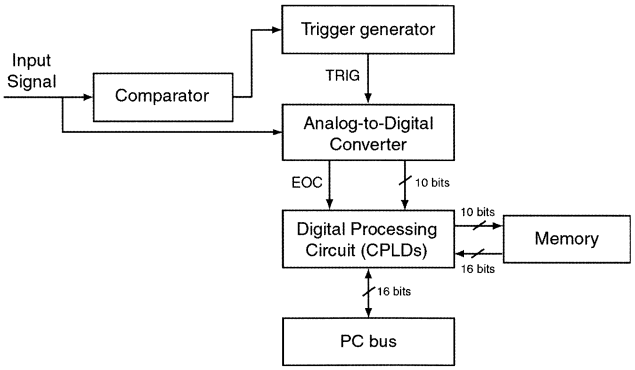


Fig. 1. Block diagram of the MCA circuit.

the ADC conversion. In the particular case of our detection system application, the width is set to 500 ns, since the TAC signal amplitude takes this time interval to reach maximum amplitude. These analog processing units are implemented on the MCA board, but are placed as far as possible from the digital circuits. In order to keep signal integrity at its best, the ground planes for analog and digital circuits are physically separated so that electromagnetic noise transmission from one to another is minimized. The comparator and trigger generator circuits are shown in Fig. 2. Once a conversion is completed, the end of conversion (EOC) signal from the ADC starts up the logic machine action in the CPLD. The first action is to latch 12 ADC bits to a static random access memory (SRAM) in the CPLD internal latches. The 20-MHz clock is then used to generate two pulses, which are sent to the READ and WRITE memory chip pins. As illustrated in Fig. 3, four clock cycles are required. At the falling edge of the first pulse, the memory address given by the 12 latched bits is read. At the rising edge of the same pulse, the memory content is incremented by one. Finally, at the rising edge of the second pulse, the incremented value is written back to the memory address. Then the circuit is free to process another event. The whole histogramming process is done by logic circuits programmed in the CPLD. The external devices needed in this configuration are only the ADC, the SRAM, and the clock. The MCA board is plugged to the ISA bus of any PC, so that the memory contents may be read via the I/O bus. I/O instructions are written in assembly sub-routines, while the main software code, developed in the Delphi [11] environment, deals with data display, storage, and acquisition control. The software package includes all the controls needed by the user to set the MCA operation. It also features user friendly tools to open and save files, modify graphics attributes, compare spectra, fit curves to data, etc.

III. Results

The MCA quality is primarily determined by the used ADC properties. Two ADCs have been used in order to evaluate the performance of our MCA scheme. One of these is AD976ACN from analog devices [12], a successive-approximation, switched-capacitor ADC. It features a 200-K sample-per-second (sps) sampling rate, 16-bit resolution, and $\pm$2.0 LSB DNL. This high DNL was compensated for by using only the 12 most significant bits. The other ADC is AD1671KP, 12-bit resolution, also from analog devices. It makes use of the subranging flash conversion technique [13]. This converter achieves 1.25-M sps sampling rate, $\pm$2.0 LSB DNL. In the following text, we refer to AD976ACN and to AD1671KP as ADC1 and ADC2, respectively. Both accept 0 to 10 V as input amplitude range. We have also compared the obtained performance results with the ones measured with a commercial MCA [14].

A. Data Acquisition Rate

The maximum achievable data acquisition rate was evaluated by injecting pulses at controlled rate, from a pulse generator, to the MCA input. Then, the number of counts per second registered by the MCA is plotted as a function of the input frequency. Fig. 4 shows the results for ADC1 and ADC2. As expected, the true and measured rates are linearly related up to a maximum frequency which is in agreement with the ADCs manufacturer specifications.

B. Differential Nonlinearity

By using two pulse generators and preparing two independent signals of frequency close to each other, one for the *start* and other for the *stop* TAC input, we may have the whole range of amplitudes at the output, since the TAC measures the time difference between *start* and *stop*. The step in amplitude values so generated is given by the difference between the signals period. This technique provides us with an easy way to generate homogeneous histograms, hence to measure the DNL. Fig. 5 shows one such spectrum, measured with the MCA using the ADC1. The lower plot in the figure is a close view of the spectrum, where one may see variations of the measured counts around an average value. The number of counts per amplitude value, which should be constant under perfect conditions, may be fit by a Gaussian curve. We take the standard deviation of this curve, divided by the average value, as the parameter measuring the DNL. Notice that the statistical fluctuations in every physical process imply deviations from the average. Therefore, in the evaluation of the DNL, the average number of counts, N, must be high enough so that the statistical fluctuation, $1/\sqrt{N}$, is negligible as compared to the DNL itself. The DNL values obtained, for 1024 channels, with ADC1 and ADC2 are, respectively, $2.46 \pm 0.22\%$ and $0.83 \pm 0.03\%$.

C. Position-Sensitive Detector Application

As mentioned above, our MCA was developed for application with a position-sensitive detector. An X-ray photon absorbed in the detector generates an electric charge avalanche, which induces a signal on a set of regularly distributed cathode sampling pads. Each pad is connected to a delay line cell, so that the photon absorption position may be estimated from the time taken by the signal to travel to the ends of the delay line [5]. The complete detection system setup is illustrated in Fig. 6. The DNL is a very important parameter for this application, and may be evaluated by uniformly illuminating the detector with the homogeneous X-ray source. We have used the ^{55}Fe source for this purpose. In order to verify that the proposed MCA qualifies for use in this application, we have done the same measurement

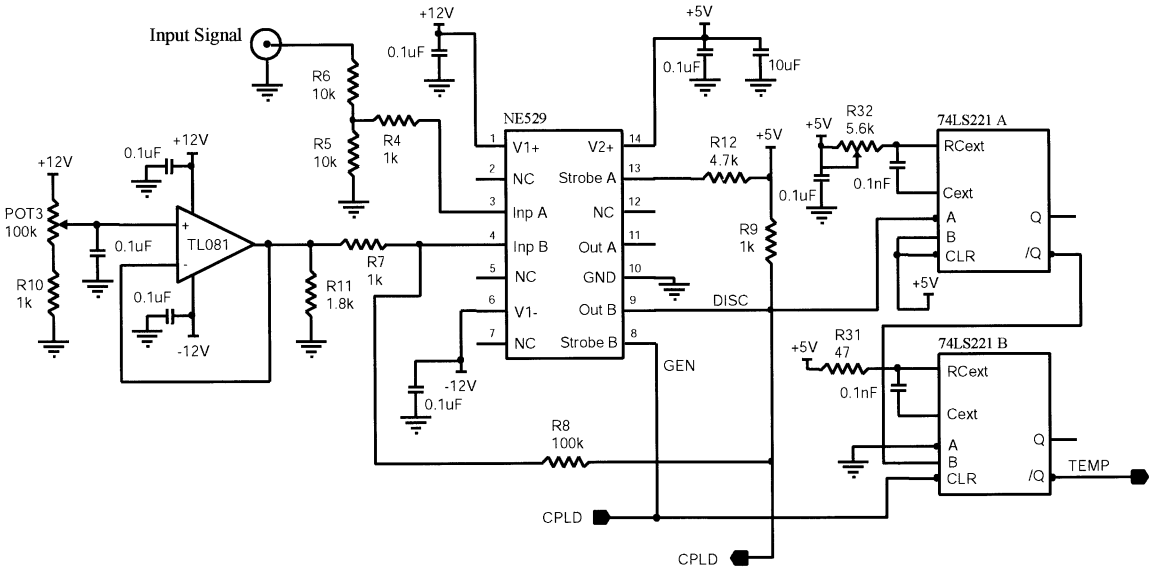


Fig. 2. Comparator and trigger generator circuits.

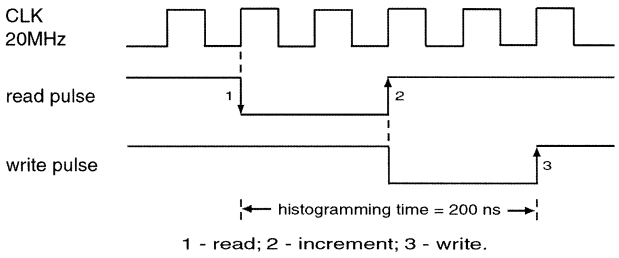


Fig. 3. Timing diagram for the state machine.

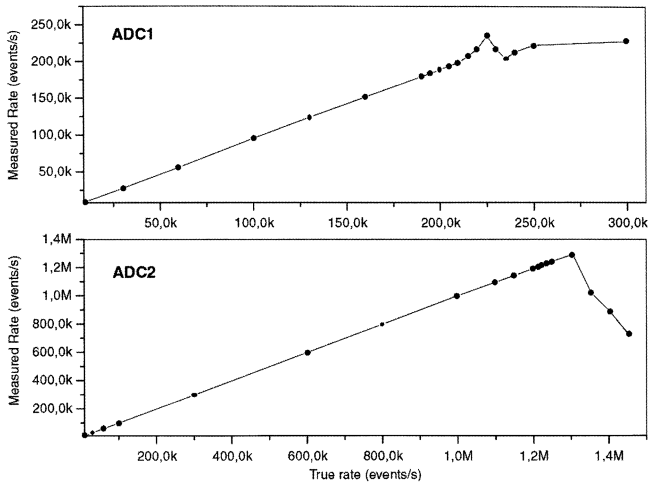


Fig. 4. Maximum counting rate of the MCA for both ADCs tested.

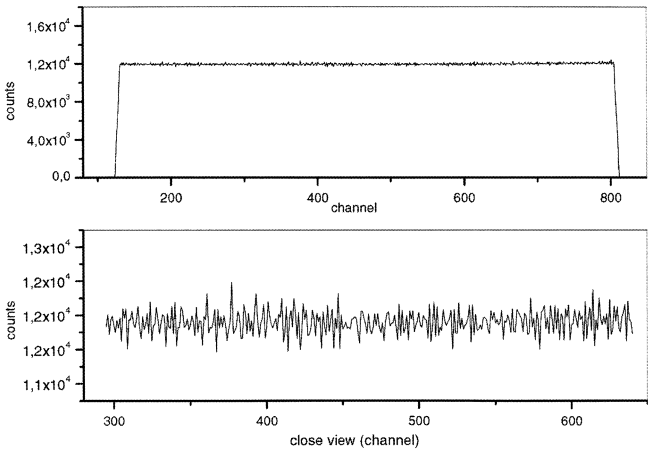


Fig. 5. Homogeneity histogram using a TAC and two-signal generators to generate the input signal.

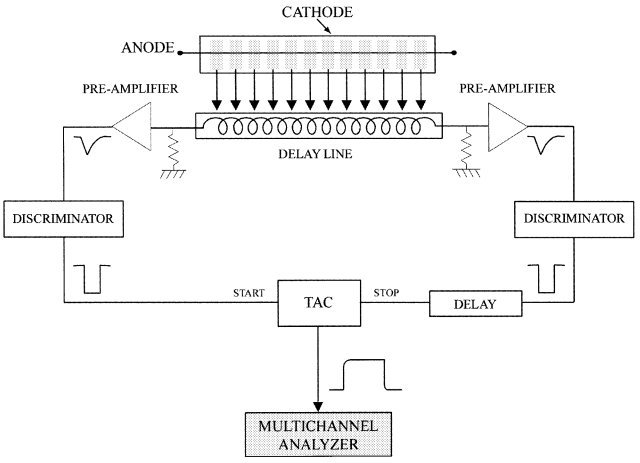
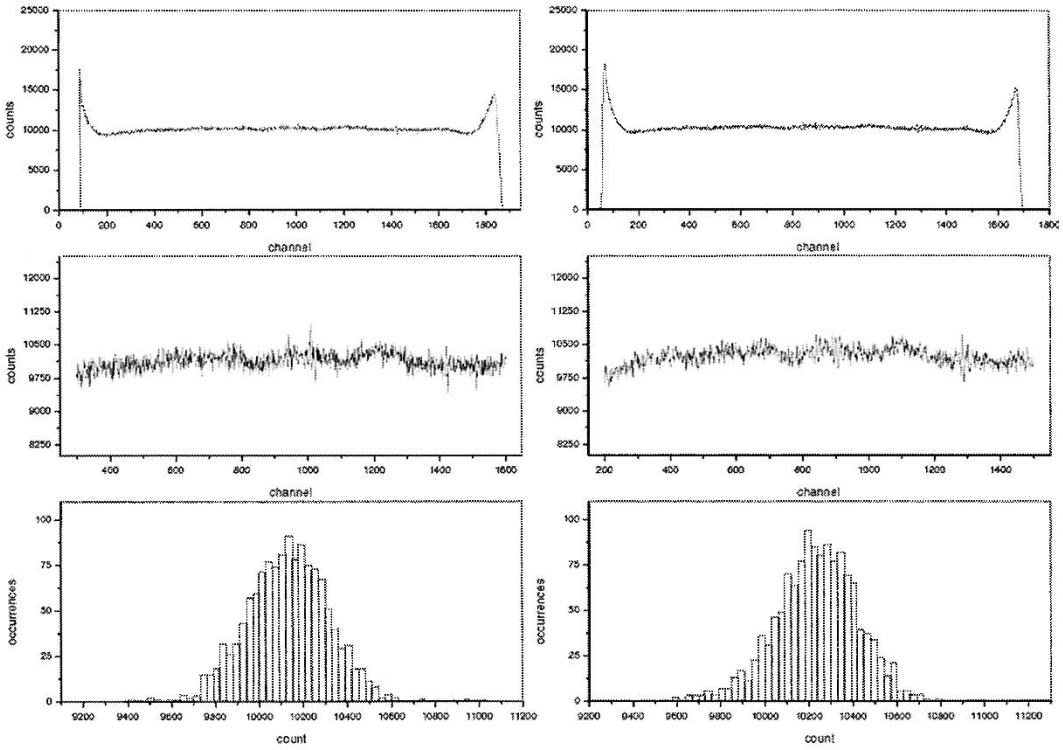


Fig. 6. Detection system setup including the detector, standard electronics, and the MCA.

with the commercial MCA previously mentioned, which features generally accepted performance parameters. Fig. 7 shows the comparison in the case where both MCAs operate with 2048 channels. The peaks at the spectrum sides are related to edge effects from the electrodes and from the delay line, intrinsic to the detector. A close view of the spectrum and the Gaussian fit to the counts distribution are also shown for each MCA. Table I summarizes the results obtained for 1024, 2048, and 4096 channels. Notice that these are DNL values for the whole detection system, not only for the MCA. It should be noted that none of the usual techniques to improve ADCs DNL [15] was implemented in the present MCA circuit.



(a) (b)

Fig. 7. Homogeneity spectrum for (a) the developed MCA and (b) for a commercial one.

TABLE I
NONHOMOGENEITY FOR THE PROPOSED MCA AND FOR A COMMERCIAL ONE

	1024 ch	2048 ch	4096 ch
Developed MCA	1.55%	1.73%	2.18%
Commercial MCA	1.49%	1.59%	1.58%

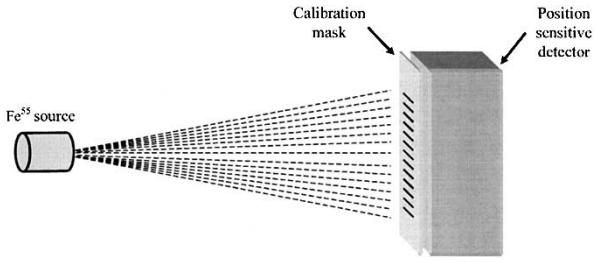


Fig. 8. Experimental setup for the integral nonlinearity measurement.

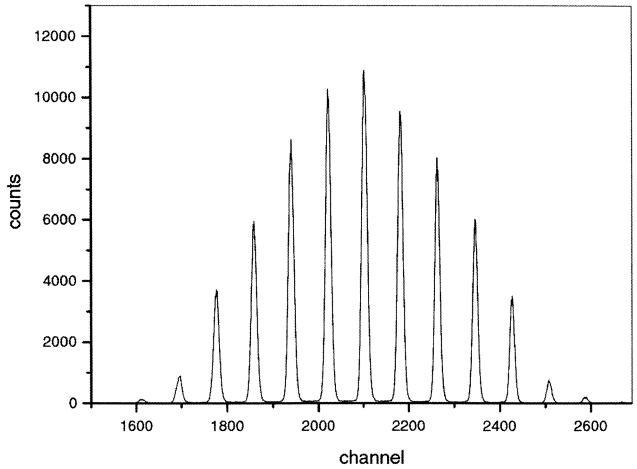


Fig. 9. Peak profiles resulting from the illumination of the detector through a calibration mask.

D. Integral Nonlinearity

The position-sensitive detection system also allows us to measure another important MCA performance parameter, namely the integral nonlinearity. A 5-mm-thick mask with regularly spaced slits is placed upon the detector window, as shown in Fig. 8. The slits width is 0.3 mm and the pitch is 2 mm. By illuminating the detector with the ^{55}Fe source, we should obtain with the MCA a set of peaks corresponding to the slits positions. The distance, in channels, between two adjacent peaks must be a constant proportional to the slits pitch. Fig. 9 is a plot of the peaks obtained using ADC1. In Fig. 10 the peak central channel (obtained by a Gaussian fit to each peak) is plotted as a function of the slit position in the mask. A linear

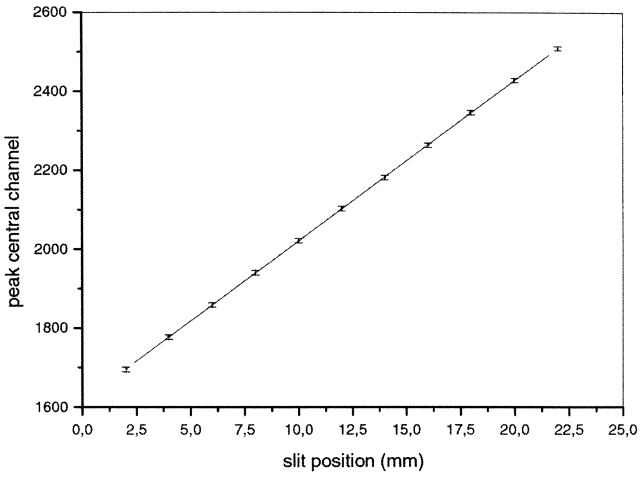


Fig. 10. Integral nonlinearity of the MCA.

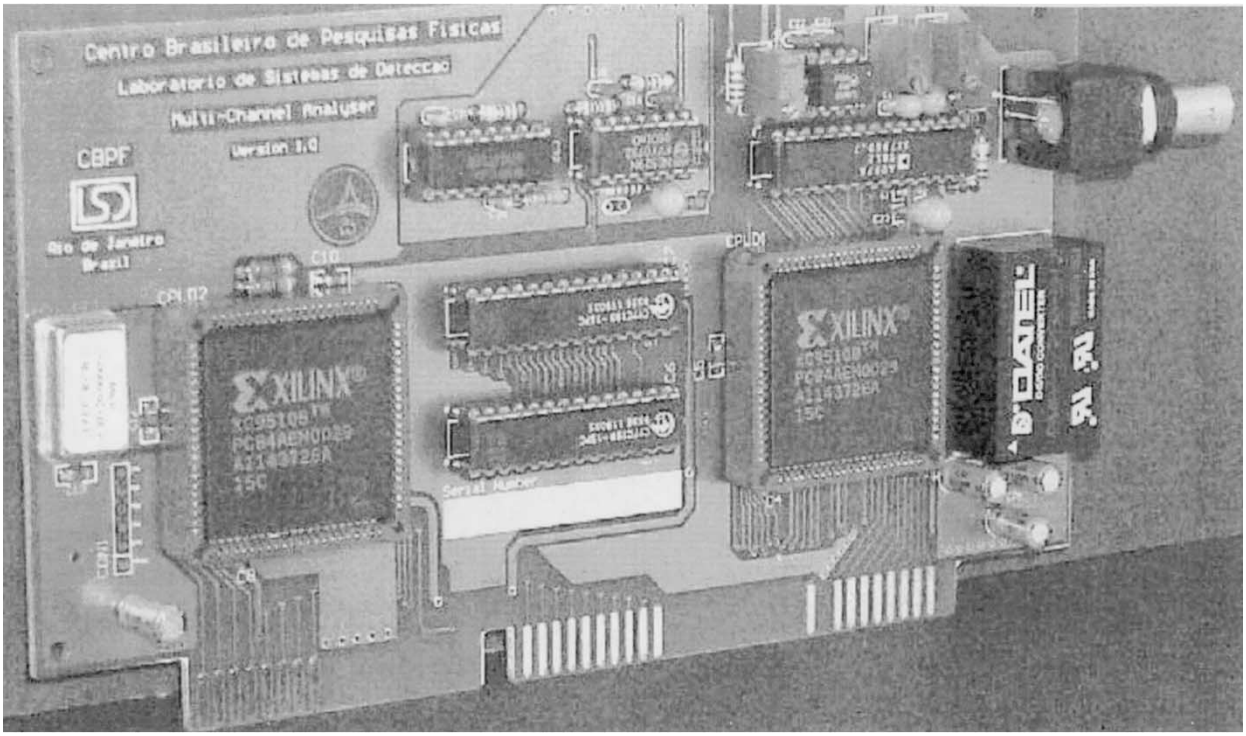


Fig. 11. Printed circuit board for the presented MCA.

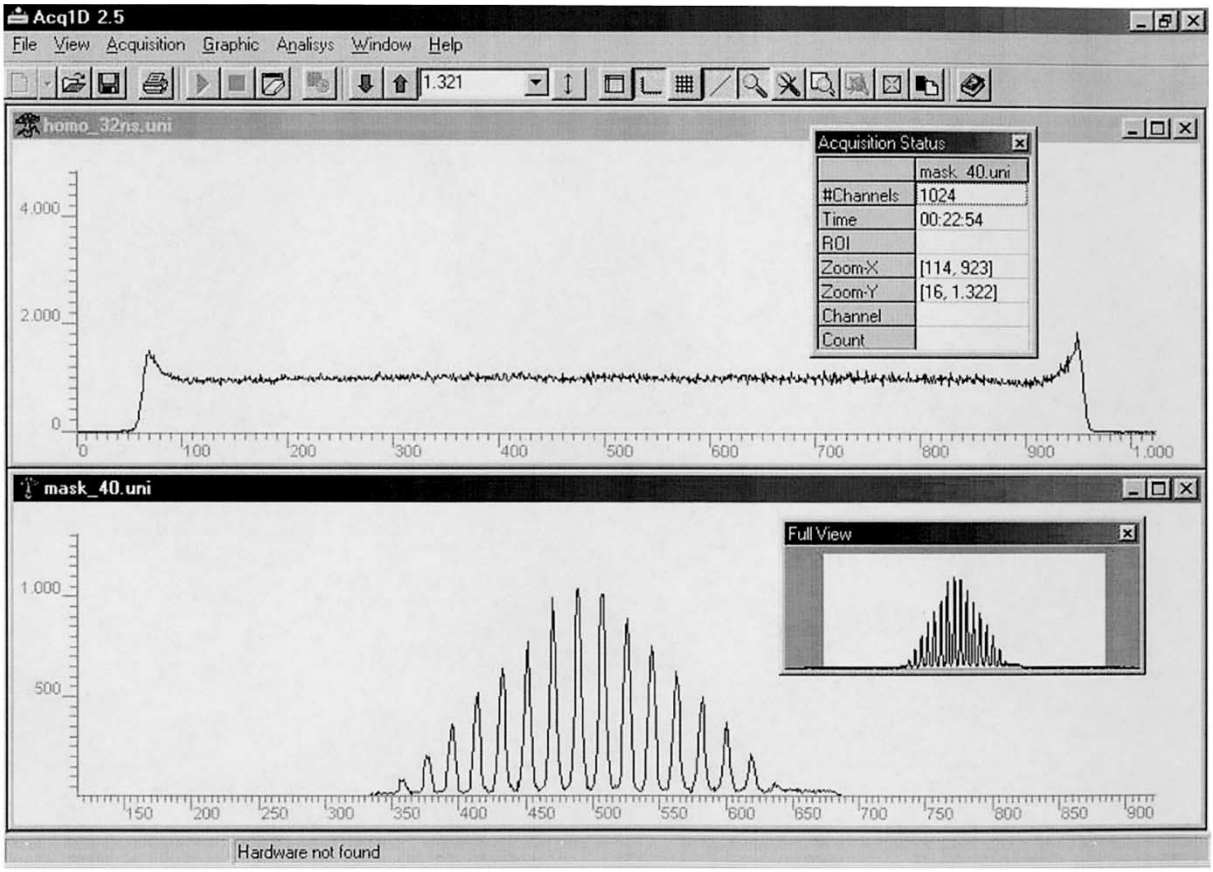


Fig. 12. User interface software for Windows OS.

fit is applied to the data. We define the nonlinearity parameter, NL, as

$$NL = \left(\frac{|Ch_{\rm lf} - Ch_m|}{R_{\rm ch}} \right) \times 100\,[\%] \qquad (1)$$

where $Ch_{\rm lf}$ is the channel obtained from the linear fitting on the measured points, Ch_m is the measured channel, and $R_{\rm ch}$ is the effective range of channels used in the experiment. The NL value obtained for the MCA operating with both ADC1 or ADC2 is below 0.1%.

IV. Conclusion

A new, fast MCA has been developed. The design is based on the most used topology in the field, but it uses programmable logic devices instead of a microprocessor, achieving competitive performance, especially for high counting rate applications. The proposed system features 200-ns intrinsic dead time with a 20-MHz clock. It should, therefore, be able to process up to 5-MHz data acquisition rate, although it is presently limited by the conversion time of the used ADCs. The obtained results are comparable to those obtained with commercial MCAs which use microprocessors or microcontrollers. Other ADCs may be easily incorporated to the design, allowing for the MCA to be customized according to, for example, the data acquisition rate or differential nonlinearity requirements. The production cost for the device is quite low, possibly much lower than the ones presently available in commerce. Fig. 11 is a picture of the circuit board for the MCA here presented. Fig. 12 is a hardcopy of the corresponding user interface software on the PC screen.

Acknowledgment

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