Low Speed Fiber Optic Link

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This document describes the design of a low speed fiber optical link. It discusses the main issues in the fiber optic system design and proposes options to be implemented in the D0 Silicon Readout.

1.Introduction

A fiber optic system offers many advantages over copper wire systems. The fiber used to transmit information is glass not metal, so fiber optic systems offer immunity from electromagnetic radiation and lightning. The fiber is lightweight and has small size, advantages in such applications as aviation, and the higher bandwidth allows more information to be sent per unit of time. Fiber optics also offer longer distance capability and better signal quality.

In a fiber optic system, digital data is represented by bursts of light from a laser diode or a LED(light emitting diode). This light is channeled by the fiber to a PIN photo diode at the receiver . Because light effects the reverse current flow though PIN photo diode, a transimpedance amplifier is required to convert this current to voltage and boost the signal. A quantizer circuit squares the signal and conforms to standard interface levels.(ECL or TTL).

2.Design Issues

Fiber optics is not a perfect interface. The signal level can be attenuated by insertion loss at the transmitter and the receiver, connector loss and transmission loss. These losses limit the maximum length of the fiber and affect the requirements of the transmitter and the receiver. In order to accommodate a worst case situation, a power budget should be developed so that the minimum circuit performance levels can be ascertained. A power budget is a mathematical representation of the optical power in a fiber optic system. It accounts for connector losses, attenuation due to fiber length, the minimum amount of power that should arrive at the receiver in order to guarantee a determinate B.E.R (Bit error Rate), and a safety margin defined by the designer.

The data format is important since it affects the bandwidth and the duty cycle which the interface must accommodate. There are many ways to code data in a serial format. Some allow unlimited consecutive symbols while others not. Those that do

not are called Run-Length-Limited. A fiber optic system which incorporates AC coupling can only pass RLL codes. The particular run-length-limited code must be considered carefully since it will affect the bandwidth of the system.

The optimum bandwidth of the system has to be chosen taking in account four conflicting concerns: noise, inter symbol interference, power and bit error rate.

If an interface were designed with a 3dB bandwidth equal to the minimum bandwidth for a given data rate (considering two symbols per cycle), level transitions would be smooth, like a sine wave. This is not desirable for a digital signal. Also smooth rise and fall times will cause interference between adjacent symbols resulting in a distortion of the output signal. This is known as inter symbol interference. A fiber optic interface with a higher bandwidth will have faster rise and fall times and less inter symbol interference. On the other hand, a higher bandwidth will increase the noise in the output signal.

3.Fiber Optic Circuits

Fiber optic components can be divided into three categories based upon the level of functional integration of the optical source, the photo detector and the associated circuitry.

The first group is a complete functional module supplying an electrical or optical output given the specified electrical or optical input signal. Power and data are the only concerns left to the designer. Functional modules are typically TTL or ECL logic compatible (the ECL compatible logic is used for data rates above 50 Mbauds per second). The second group is a group of components which are incorporated into a single package to provide a particular function that is generally difficult to achieve by the system designer. The third group is a set of discrete components, where each one of these will perform a portion of the system. Circuit design must be provided. Table 1 gives examples and states comparisons between them (Ref. 2).

Group	Example	Board space	Circuit Design	Cost
I	Integrated modules	Lowest	Lowest	Highest
II	Pin transimpedance Amplifier	Medium	Medium	Medium
III	LED, transistors gates	Highest	Highest	Lowest

Table 1.

4.Transmitter Design

The light source can be either a LED or a laser diode. LED are multimode light emitters and as such they suffer a higher level of chromatic dispersion, caused by different propagation velocities of light at different wavelengths, than the laser diodes. This is the dominant bandwidth limiting factor for LED driven fiber optics links. Light emitting diodes have a spectrum on the order of 40 to 60nm full width at half maximum amplitude centered at 820 nm. On the other hand LEDs are cheaper than laser diodes and can be modulated in the 100 MHz range, making them suitable for short to medium distance communications.

From the specifications listed above, one can see that LEDs are suitable for the design of the low speed link. Table 2 shows a list of some LEDs and their characteristics.

LED	Rise time (ns)	Power Output(μW)	Manufacturer
MFOE1203	2.5	40	Motorola
HFBR1414	3.0	44.6	Hewlett Packard
1A277	2.0	50	ABB-Hafo

Table 2.

LEDs are current driven devices so a current modulator is needed to use the LED as a data transmitter. To obtain the best performance from LED and driver combination, two simple techniques known as prebias and drive peaking should be employed. Prebias, as its name implies, is a small forward current applied to the LED in the "off" state, thus reducing the amount of charge that the driver must transfer to turn the emitter back on. Peaking is a momentary increase in the LED forward current that is provided by the driver during the rising and falling edges of the pulses that are used to modulate the emitter. If the time constant peaking is approximately equal to the minority carrier lifetime of the transmitter, the momentary increase in LED current will transfer charge at a rate that improves the rise and fall time of the light output without causing excessive overshoot(Ref.2, 3).

5.Receiver Design

The dynamic range must be large enough to accommodate all the variables a system may present such as LED output variation, LED driver variation, thermal variations, etc.

The receiver must have a a high sensitivity since the power of the signal that comes from the fiber is in the order of a few microwatts. In order to improve the sensitivity, receivers usually include an AC coupling. Filtering the excess of bandwidth is also another precaution to improve sensitivity(Ref. 3).

The bandwidth has to be enough for the data rate chosen and interface with standard interfaces must be provided. Another feature that sometimes is desirable is the Link Monitor. This circuit monitors the input level and sets a flag and/or disable the digital output when the inputs falls bellow a predetermined point.

Specifications for the low speed data link

The low speed link is intended to be used to send a 53.1 MHz clock and commands from the VME SAR board to the Port card. The approximate link length is 60 meters. There will be two lines: one for a 53.1 MHz clock, so in this way all the data acquisition system runs synchronous, and the other for data (Ref. 1).

The data format for the data line is shown in the table 3.

Bit 0	Bit 1	Bit2	Bit 3	Bit 4	Bit5	Bit 6
framing	crossing	Data 3	Data 2	Data 1	Data 0	Parity

Table 3.

The use of the parity bit and choosing carefully the codes for the most frequent commands are two precautions that have to be taken to avoid long sequences of zero's or one's. These low or high duty cycles are not desirable since they allow parasitic capacitance in the receiver and the transmitter to charge. The time required to charge and discharge undesirable capacitance in the transmitter and receiver result in a pulse-width distortion related to the instantaneous duty cycle of the data.

The bandwidth for the system has to be chosen in order to accommodate a maximum data rate of approximate 106 Mbauds per second for the clock line and 53 Mbauds per second for the clock.

Design of the low speed link.

The first thing has to do is write the power budget for the link. The power budget can be expressed by the formula below:

$$P_t \geq \alpha_c + \alpha_f L + P_r \qquad (1)$$

where,

P_t = Output power of the transmitter (dBm)

α_c = Total attenuation due to connection loss (dB)

α_f = Fiber attenuation constant (dB / km)

L = Fiber length (Km)

P_r = Power received to guarantee BER (dBm)

The power received to garantee a certain BER has to be a number of times greater than the "noise floor" power in the receiver. The design will be continued assuming the following:

- The light source is the 1A277 , a 850 nm LED whose characteristics are shown in the Table 2.
- The fiber is a multimode graded-index 62.5/125 μm assembled in a 60 m Accuribbon cable (AT&T) terminated with Mac II connectors (AT&T) and 1m jumpers terminated with ST connectors in one side and Mac II connectors in the other.

Tables 4 and 5 show some characteristics of the fiber and the connectors (Ref. 5).

Bandwidth	160 MHz/Km @ 850nm 500 MHz/Km @ 1300nm
Attenuation	3.75 dB/Km @ 850nm 1.0 dB/Km @1300nm

Table 4.

Connector Type	Attenuation
Mac II	0.7 dB (typ) 1.4dB (max)
ST	0.3 dB (typ) 1.0dB (max)

Table 5.

From the equation (1) and using the values in Tables 2, 4 and 5 :

$$P_r = -18 \text{ dBm}$$

If the BER desired is 10^{-12}, this means that the "noise floor" in the chosen receiver has to be (Ref. 6):

$$P_{nfr} \leq P_r - 10\log\left(\frac{14}{1}\right) \text{(dBm)}$$

$$P_{nfr} \leq -18 - 11.5 = -29.5\text{(dBm)} \quad (2)$$

6.Bandwidth

As it was said before the choice of the correct bandwidth is related to noise, inter symbol interference, power and BER. When one combine these conflicting concerns, the optimum bandwidth is ideally constrained in the range between 0.6 and 0.8 times the signaling rate in baud (Ref.3). So for 106 Mbauds, the bandwidth required would be in the range 63.6 - 84.8 MHz. It's important to note that if the amount of optical power that can be delivered at the receiver is greater than the minimum required to guarantee a given BER, one can use more bandwidth and provide faster rise and fall times, decreasing the amount of inter symbol interference.

7.Circuit Implementation

7.1.Transmitter

The LED driver is usually implemented by high current line drivers. This can be implemented by using ordinary gate and discrete transistors.

A better approach is the use of drivers such as 74F5300 or 74F3037. Since they have high output current capability, the transistor buffers are not required, only a few resistors and capacitors for pre-bias and peaking, respectively.

Another possibility of implementation is the use of LED drivers such as UCP1648(NEC). They reduced the number of discrete parts to a minimum, reducing the board space and increasing reliability and the designer have the choice of the LED(usually integrated modules use 1300nm parts that are more expensive).

The last would be used integrated modules. They are rated to 50,70,125,200,266 Mbauds and come in a 16 DIP package with connector included (so the designer does not have to worry about mechanical placement of connector). There were selected the ST-1040-125 (BT&D) for the clock line and the ODL 70 (AT & T) for the data line.

7.2.Receiver

The four major blocks of a receiver are the optical to current conversion, the current to voltage conversion, the analog to digital conversion and the link Monitor.

The first two blocks will be implemented using a PIN diode and transimpedance amplifier. There are several manufactures of discrete PIN photo diodes and transimpedance amplifiers. Some of these manufacturers offer both functions in a single module with fiber optic connectors, like the HFBR-2416. These modules isolate the most noise sensitive section of the receiver, the photo diode to the transimpedance amplifier connection, and protect it from outside influences. In

addition they are relatively low cost and eliminate the need to design fiber optic connector hardware. The HFBR-2416 also has a "noise floor" lower than the quantity stated in equation (2).

The output of the HFBR-2416 is a low level analog voltage which is proportional to the incident optical power. It needs to be amplified, square-off, and appropriated level shifted to a standard interface (TTL or ECL). This is all done by the ML6622 or ML4621 from Microlinear. They also include a Link Monitor feature (Ref. 3).

The other approach is use the integrated modules. They have similar characteristics of their transmitter counter parts.

8.Experiments and results

In order to implement what was discussed in the previous sections, some prototypes were built and the performance evaluated.

8.1.Test setups

The Figures 1 and 2 show the setups that were used to evaluated the transmitters and receivers. A pseudo random bit sequence was used as the input of the link and the eye pattern was observed, both in the output of the transmitter and the receiver.

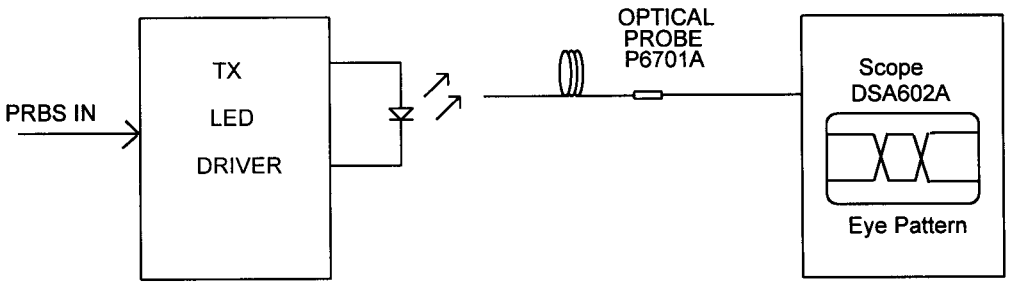

Figure 1. Test setup for optical transmitters

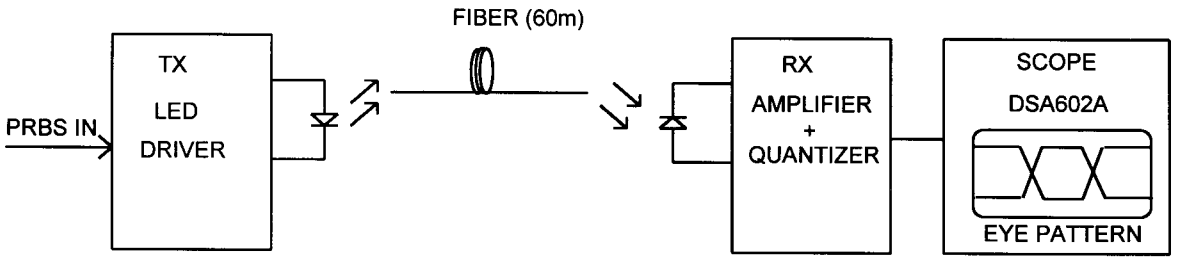

Figure 2. Test setup for the optical link

A pseudo random pattern provides a better way to evaluate the link, than a 1010 pattern at the same data rate, because they better simulate real data being transmitted. They also expose the link to low and high duty cycles, allowing parasitic capacitances to charge in the receiver and in the transmitter. The time required to charge and discharge those capacitances can introduce pulse width distortion. Low and high duty cycles can also affect the sensitivity of AC coupled receivers.

8.2.Data line

The circuit implemented to transmitter for the data line is shown in the appendix A. This circuit uses an IC driver and a few resistors and capacitors to provide the prebias and peaking. This driver is very low cost and it bandwidth is suitable for operation at 53 Mbauds range. A $2^7 - 1$ pseudo random bit sequence at 50 Mbauds/s and the eye pattern can be seen in the figure 3.

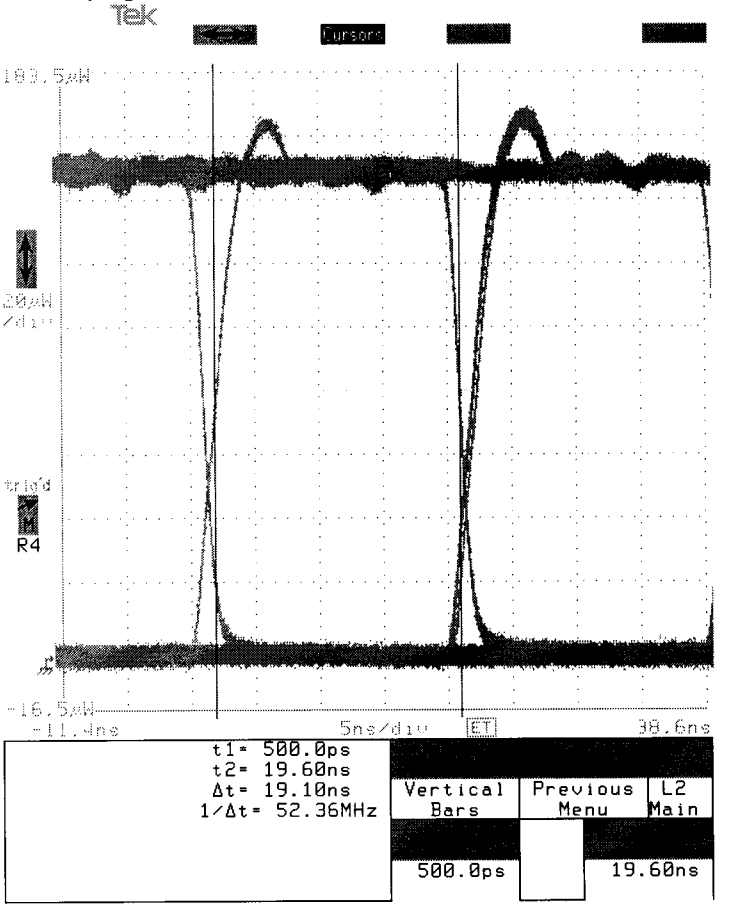

Figure 3.Eye pattern @ 50Mbauds/s (5ns/div) - transmitter.

The crossings of rising and falling are shifted away from the 50% level. This indicates that the transmitter introduces some pulse width distortion .

Figure 4 shows the eye pattern of the data line in the output of the receiver . One can see that the receiver also introduces pulse width distortion. For the date line the total pulse width distortion is around 5%.

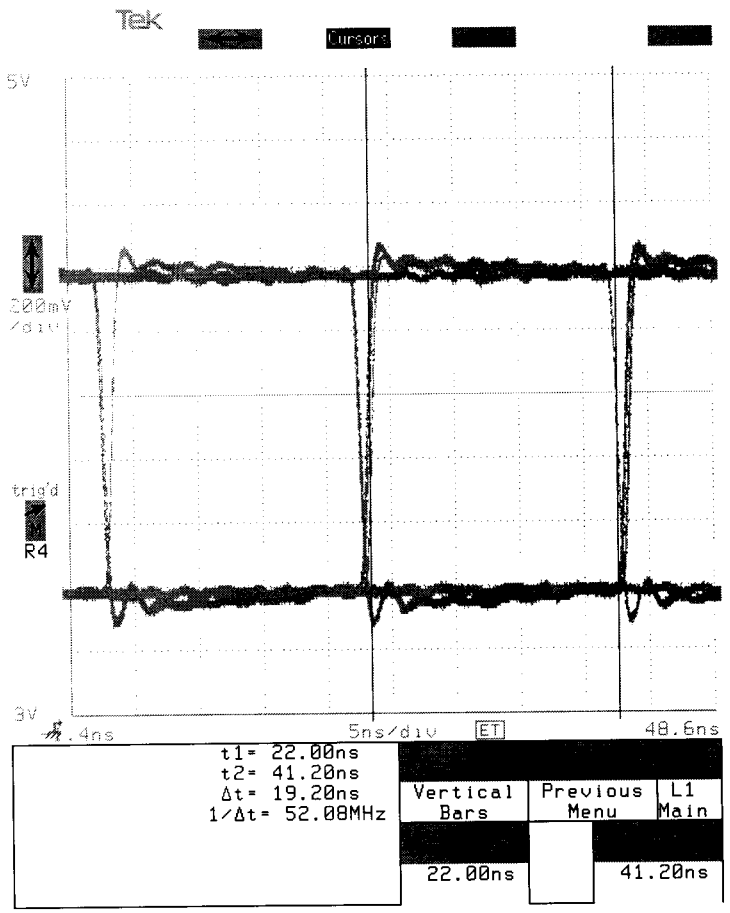

Figure 4. Eye pattern @ 50Mbauds/s (5ns/div) - receiver.

8.3.Clock Line

The circuit implemented to transmitter for the clock line is shown in the appendix. This circuit uses a high performance current driver to provide faster edges speeds than the ones provided with the previous circuit.

Although the clock line will always transmit a 1010 pattern at 106 Mbauds per second, a $2^{20}-1$ pseudo random bit sequence was used to evaluate the performance of the clock line under more severe conditions. The eye pattern can be seen in the Figure 5.

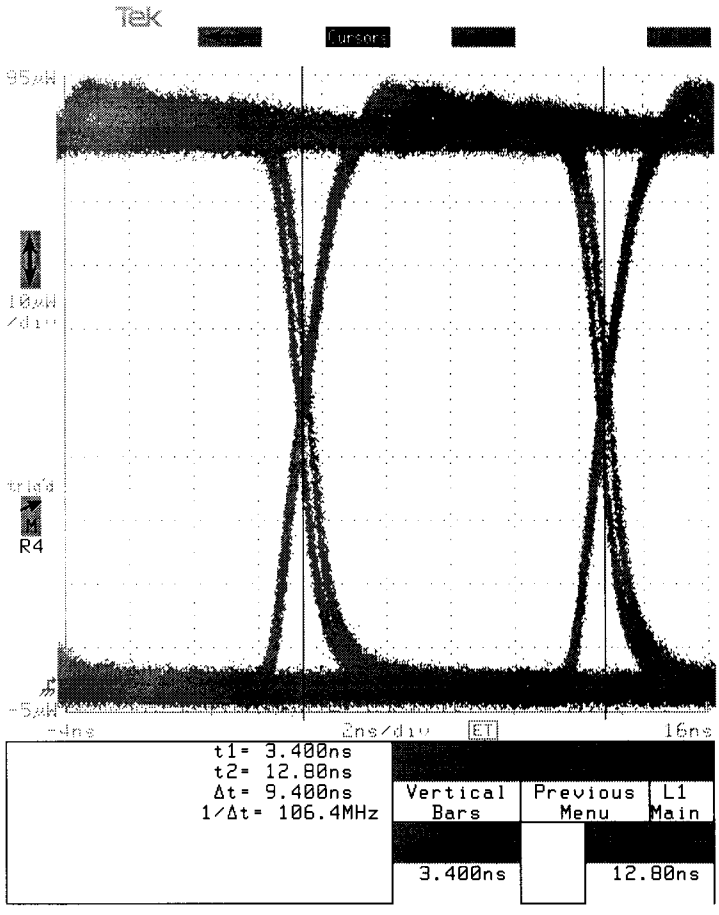

Figure 5. Eye pattern @ 106 Mbauds/s(2ns/div) - transmitter.

In this case the amount of pulse width distortion in the wave form is much smaller.

Figure 6 shows the eye pattern of the clock line in the output of the receiver. The amount of pulse width distortion has increased but is very low in the order of 1%.

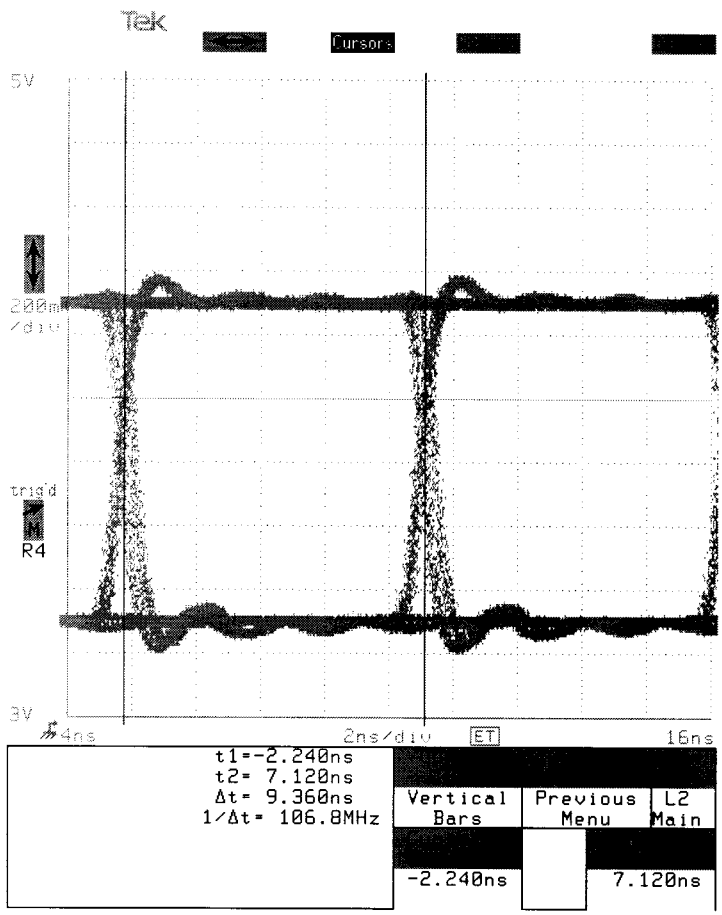

Figure 6. Eye pattern @ 106 Mbauds/s(2ns/div) - receiver.

The performance of the integrated modules was also evaluated. A $2^{20}-1$ pseudo random bit sequence and the eye pattern can be seen in the Figure 7.

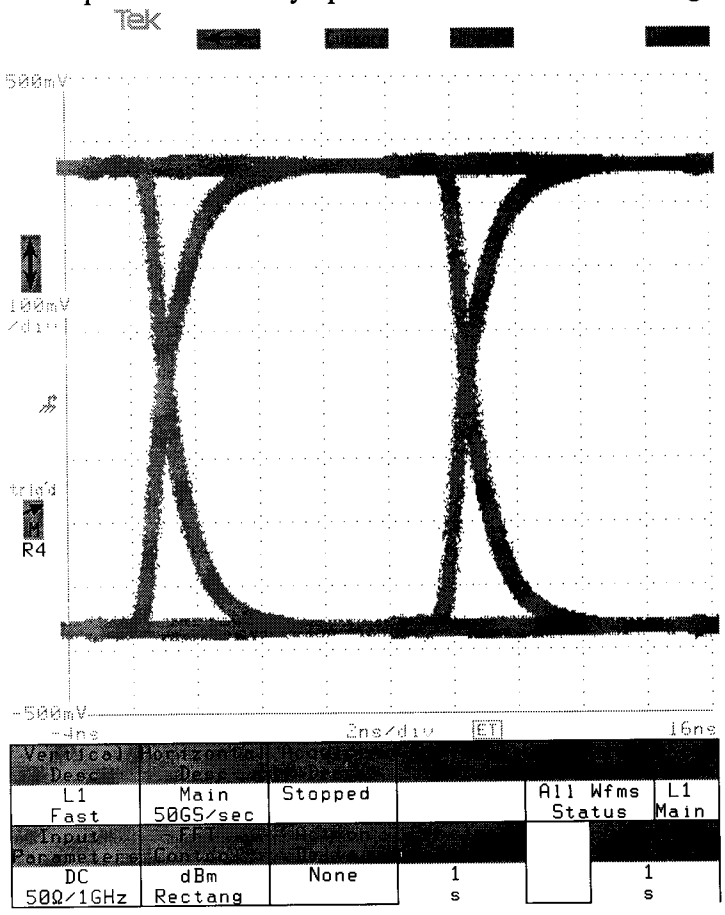

Figure 7. Eye pattern @ 106 Mbauds/s(2ns/div) .

The pulse width distortion is very low and the eye pattern is wide open.

In order to obtain the waveforms displayed here with rise times in the order of 1 ns, it is very important to observe a good construction and layout practice. Excessive amounts of parasitic inductance or capacitance will degrade the stability and the bandwidth of the link. Surface mounted components are recommended.

From the circuit implementation options and the results presented, the best choice to implement the low speed line are the discrete circuits shown in the Appendix . They do offer similar performance of the integrated devices at a fraction of the cost. They also provide more flexibility for future upgrades. Table 7 summarizes the components used.

Line	Tx	Rx
Data	74F5300+ 1A277	HFBR-2416+ML6622
Clock	UCP1648 +1A277	HFBR-2416 +Ml6622

Table 7.

9.Conclusions

The design of the low speed link was explained in detail. Circuits readily available and techniques to improve performance were described. The performance of some circuits were discussed were tested and analyzed in according to the application requirements and the circuits to implement the link were proposed.

10.References

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