High Speed Optical Link

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This document describes the design of the high speed optical link. It discusses the main issues in the high speed fiber optical link design and proposes an option to be implemented in the D0 Silicon Readout.

1 Introduction

Transmitting a great number of data channels always has been difficult. The amount of cable involved to transfer each data channel individually is very large. This can be not only costly but also impractical due to space constrains. This situation can be even worse if the data channels are not independent, but part of a parallel data word. In this case not only the problems mentioned before occur but one also has to ensure that all the parallel data word arrives at its destination with minimum timing skew between each line. Expensive shielded ribbon cable should be used to in order to minimize the Radio Frequency (RF) radiation from the cables. Crosstalk between lines is another real possibility.

Transmitting the data in a serial format rather than parallel form can reduce the above problems. In serial form the data can be transmitted using coax or fiber optic cable. Fiber is the choice when one is looking for a system immune to electromagnetic interference and does not want to have RF radiation emanating from the cable. Fiber is also lightweight and takes less space.

The serial approach has been used for a long time in telecommunications industies. The telecommunication industry had the need to move large number of low speed data streams (typically digitized voice channels) over long distances. The solution was to multiplex many of the low speed data streams to form very high speed serial data streams. Fiber optics are used to send these high speed data streams over long distances.

Other information intensive industries are starting to use high speed optical links to solve their data transport requirements. Most notably the data communications and broadcast industries. While the data transfer requirements are similar to the requirements of the telecommunication industry, many of these applications require short transmission distances when compared to most telecommunication applications. This will make that design choices made for a high speed link for telecommunications may not be the best for a high speed link for data communications.

2 Design Issues.

The length of the link plays an important role in the terms of the choice of fiber to use. For applications that require more than 1 Km transmission distance, single mode fiber is used. However for applications with less than 1 Km transmission distance, multimode fiber is useful in several applications. One key motivation is the installed base of multimode fiber. The widespread availability of 62.5/125μm " FDDI-Grade" fiber makes it an attractive option for many short range applications.

Other important variables are the operating wavelength and the type of light emitter. The options are "CD" lasers at 780 nm and 850 nm, more conventional 1300nm and 1550nm lasers and even light-emitting diodes.

Recently "CD" lasers started to be used to implement low cost high speed links. However they have serious problems when working with singlemode fiber because it is actually bimodal at "CD" wavelengths. This reduces the bandwidth and increase the modal noise. The other negative aspect is that many singlemode fibers are not rated to operate at these wavelengths. "CD" lasers are best suited for use in short range applications with multimode fiber. They offer high power, high speed and low cost.

The choice of 1550nm is not very attractive due to the cost of the devices at these wavelength. This choice is only justified when the ultra-low loss that can be achieved with those devices is needed.

The choice of light-emitting diodes (at any wavelength) is possible only at low data rates. Data rates above 300-400Mb/s are difficult to achieve with light emitting diodes. While there are some papers reporting tests achieving data rates above 1 Gb/s, they have not appeared in production links.

1300nm lasers have been used for a long time for high speed links. They have lower fiber attenuation, higher bandwidth and true singlemode operation in singlemode fiber. Their price is, however, higher than CD lasers.

The Table bellow summarizes the characteristics of the light sources.

		Single mode fiber			Multimode Fiber		
Light emitter	Emitter Cost	Fiber Loss	System Bandwidth	Overall Performance	Fiber Loss	System Bandwidth	Overall Performance
780 nm	Low	High	Moderate	Fair	High	Moderate	Good
850 nm	Low	Moderate	Moderate	Fair	Moderate	Moderate	Good
1300nm	Moderate	Low	High	Excellent	Low	High	Excellent
1550nm	High	Very low	High	Excellent	Low	High	Very good
850nm LED	Low	N/A	N/A	N/A	Moderate	Low	Fair
1300nm LED	Moderate	Low	Low	Fair	Low	Low	Good

Table 1: Characteristics of the light sources (Ref. 2.).

3.Specifications for the high speed data link.

The Figure 2 shows a block diagram of the D0 Silicon Vertex Detector(Ref. 1).

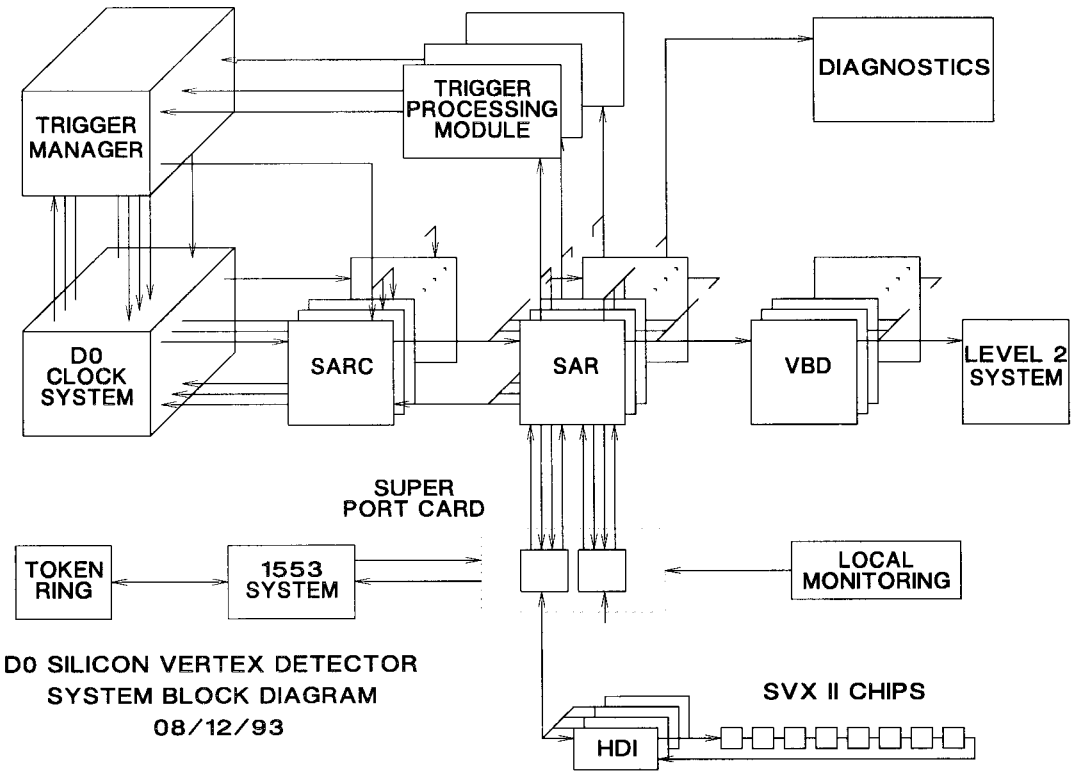

Figure 2: D0 Silicon detector block diagram.

A custom chip called SVX-II will acquire the data from the silicon-detector and will output the acquired data on a 8 bit bus at 53 Mbytes/s. A flexible printed circuit board (HDI) carrying up to 10 SVX II will transfer the data to a Port Card. There will be up to four HDIs per Port Card. The interface between the Port Card and the Silicon Acquisition Board (SAR) will be done by two Optical links . The first one is the Low Speed Optical Link, it will be used to send control and protocol information from the SAR board to the Port Card. The other link is the High speed Optical link that will be used for sending control and data to the SAR module.

The serial data rate (SDR) per HDI can be calculated by the equation bellow:

$$SDR = .\frac{8bits}{byte}.53Mbytes/s$$

SDR = 424 Mbit / s (data only)

Since each link will handle data from 2 HDI's, it will have to support data rate in the order of Gigabits per second.

4.Implementation

The major drawback for serialization is the high frequency circuit required. As it was said before, the circuit has to support a data rate in the order of Gigabits plus any overhead for error detection and synchronization.

There are several manufacturers of high speed parallel to serial chips, most of them are designed for implementation of standards such as HIPPI or Fibre Channel, which means fixed bus wide and clock speed. Another disadvantage of such chips is that designer of proprietary links has to live with built in protocols.

The Hewlett-Packard' HDMP-1000 (G-Link) gigabit-rate chipset (transmitter and receiver) offers some advantages over chips mentioned above for the high speed link . The chipset can take a 16 or 20 bit parallel word and transmit it serially. Data rates can be selected over a wide range up 1.5 Gb/s(Ref.3,4.5).

In normal operation the transmitter chip(TX) locks to a user supplied frame clock and multiplies it to produce the high speed serial clock . When locked, TX indicates that it is locked by asserting the LOCKED output. When the Enable Data (ED) signal is asserted, usually by the given state in the receiver chip (RX). the TX asserts the Ready for Data (RFD) signal indicating that is now ready to transmit data or control frames.

The interface with the TX is simple. The control signals and data input are latched on the rising edge of the frame rate clock (STRBIN). To send data, one has to check if the link is established, put the data on the bus and deassert the Data Available (DAV*) signal with the proper setup and hold times in relation to STRBIN. Similar procedure is done when one wants to send control frames, only in this case the Control Available (CAV*) signal is deasserted. When DAV * or CAV * are not active and the link is established, Fill frames are sent.
At the receiver end, RX demuxes the serial data back to its original parallel form. The interface with the RX is simple. The RX can distinguish between the various types of frames and activate the correspondent signal to a certain frame. A built in State machine controls several functions in the RX and also provide the status of the link.

The G-link will be working in "pseudo simplex" (Figure 2.). In this mode information about the status of the receiver (STAT1) is sent back to the transmitter through a low speed line. So when the receiver loses the capability of extract clock reference from the incoming serial data (lock), the information is sent to the transmitter which will execute the following sequence. The Port Card pulls the ED low and TX sends Fill Frame pulses to re-lock the receiver.

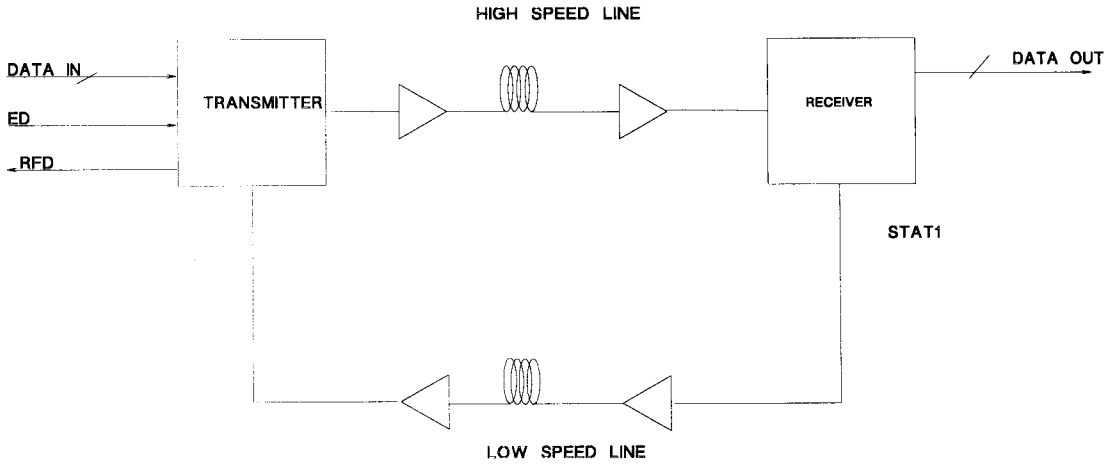

Figure 2: Pseudo Simplex mode

The output of the G-link transmitter will be then converted from electrical to optical signal and sent though 60 meters of fiber to the SAR module where it will be converted from optical to electrical signal and used as an input to the RX chip.

Each SAR module will receive 4 high speed lines. If one adds the low speed lines, the number of fiber optical cables goes to 12. It is very desirable to have a compact and easy-to-use system to connect the fiber cables with the electro-optical devices. The Accuribon cable with MAC II connector (AT&T) provide an extremely compact system that can handle up to 18 fibers. Another advantage of this assembly is that the MAC II connector already have a well developed connection to electrical backplanes providing a easy way to accommodate electrical and optical signals in a VME backplane (Ref.8).

Since the distances are very short, multimode fiber and short wavelength lasers will be used. This combination provides a low cost and high performance link. The short wavelength lasers chosen were the Finisar modules (Ref.6,7). These modules are low cost and high performance. The transmitter comes with an embedded controller FCC-2000 that takes care of the operation of the laser. A clock around 4 MHz is required and can be provided dividing the 53.1 MHz by 14. The following signals can be monitored by the host to ensure the proper operation of the lasers:

NAME	DESCRIPTION
LINK_STAT	Indicates that the link is up.
DLC_STAT	LED heart beat output.
OFC_STATUS	Status of Open fiber control (should be off)

Table 2: Laser Status Signal

The host can also turn off the laser and reset the controller.

There is a communication port in the FCC-2000 that makes possible read and thus monitors the various laser parameters such as temperature, the amount of power that is been launched and so on. This provides a powerful diagnostics tool. This information can be read by the 1553 and so it's possible to determine if the lasers have aged, and
locate in which part of the detector it occurred. The Communication Port has the following signals :

SIGNAL	TYPE	DESCRIPTION
SI	INPUT	Serial input
SO	OUTPUT	Serial output
SCLK	INPUT	Serial clock
CS	INPUT	Chip Select
READY	OUTPUT	Slave ready for serial transfer

Table 3: Communication Port Signals.

All the signals operate at CMOS/TTL levels.

To start communications the READY must be high , then the CS can be driven low. As CS goes low the FCC responds by making READY low .

Commands into the FCC-2000 and data out follow the same format . Clock rate for the shift register is less than or equal to 500 Kb/s . The clock is always supplied by the host and its required to shift commands in and to shift its responses out. The state of the SCLK between transmissions is high. The first falling edge of the SCLK signals the beginning of the a transmission, and data is presented at the to the SO pin. Data is captured at the rising edge of SCLK and the transmission is ended in the eighth edge of SCLK. After this is completed the CS line should be raised to indicate the end of the transaction. FCC-2000 releases the line READY as a completion of the handshake.

At the receiver side, the FCC-2000 is not necessary. The signal RX_OPT_PWR indicates that the receiver module is receiving optical power. since it's a analog output, discrimination has to be provided in order to have a digital signal indicates whether or not optical power is been received. This signal can also be used to determine if the line has been broken .

The Figure 3. shows a block diagram of the high speed link.

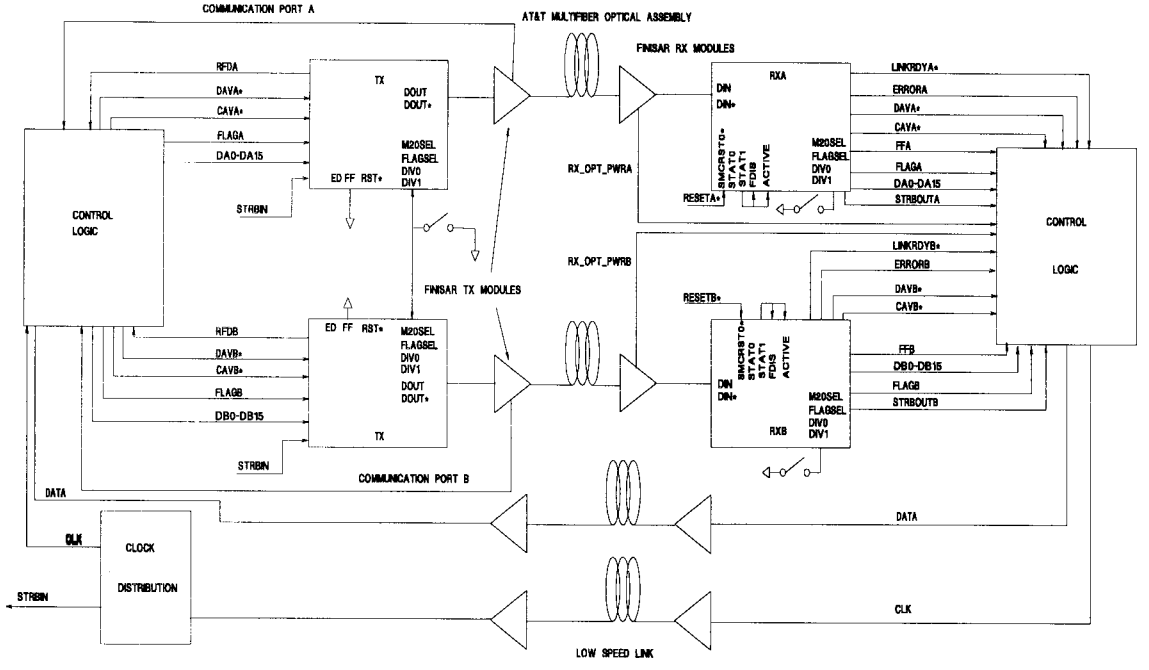

Figure 3: High speed link block diagram

5.Tests

Once the implementation was proposed some preliminary tests were made. The testing hardware used was the evaluation boards provided by the manufacturers of the
parts chosen.

5.1.Serial Bit error tester

The purpose of this test was determine if the MAC II connectors would decrease the performance of the system. The setup used is shown bellow.

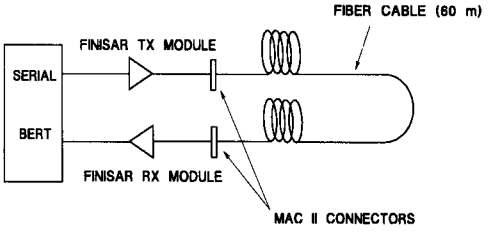

Figure 4: Bit error test setup.

The link was tested for several hours and no decrease in performance was observed.

5.2.Eye Pattern

The setup bellow was used to obtain the eye pattern of the transmission.

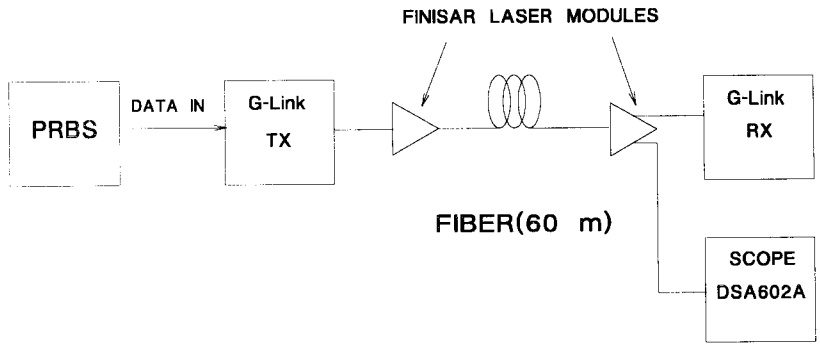

Figure 5: Eye pattern setup.

Figures 6,7 and 8 show the eye pattern at 1.2 Gb/s, 1Gb/s and 700 Mbits/s respectively.

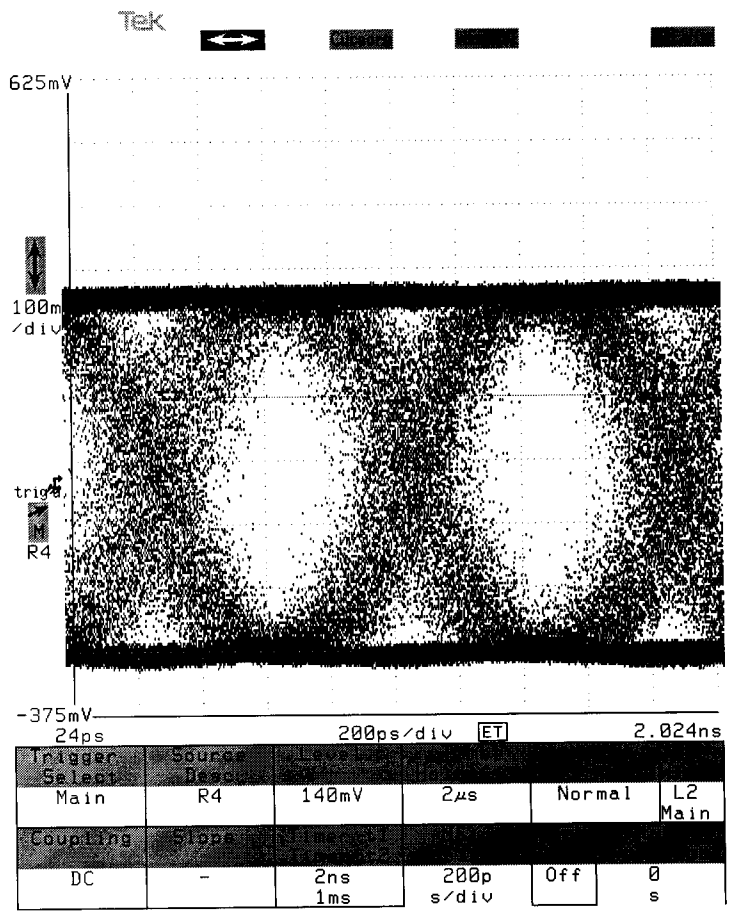

Figure 6: Eye at 1.2 Gb/s

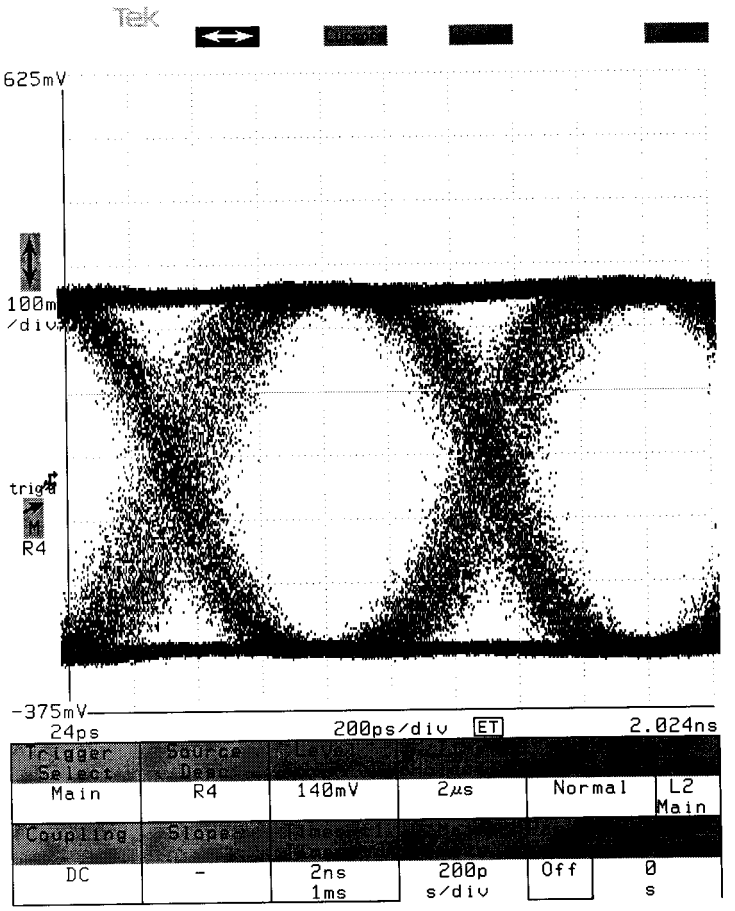

Figure 7: Eye at 1Gb/s

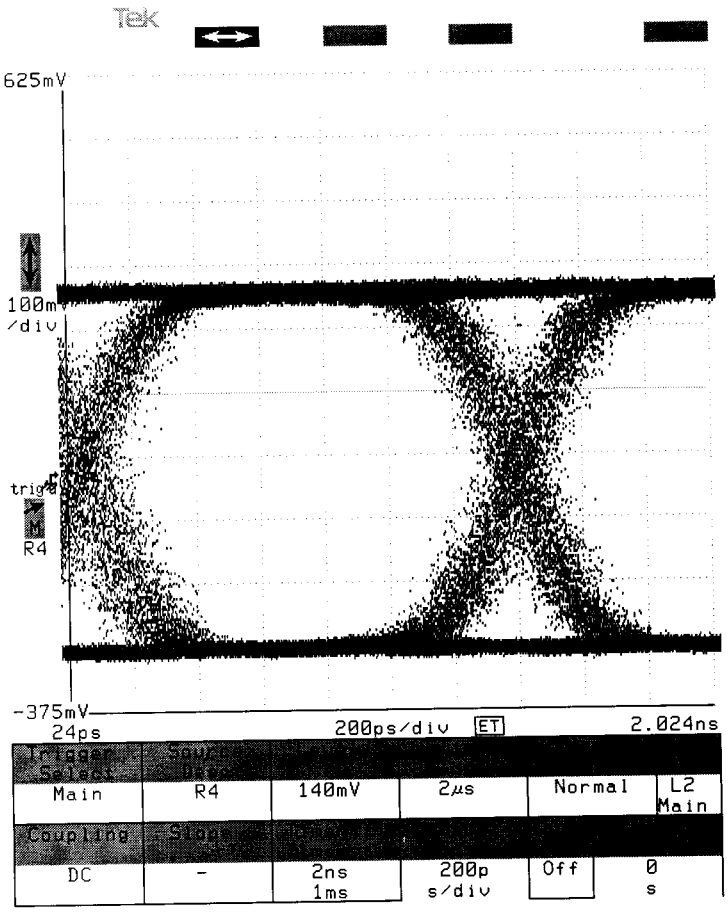

Figure 8: Eye at 700 Mbits/s

In the tests above, It is important to note that the bandwidth of the scope (1Ghz) is not
enough to accommodate all the frequency components of the serial data, so there is some signal degradation at higher rates.

5.3 Pattern Generator

A third test was made using the setup bellow. The pattern generator was used to exercise the handshake between a host and the Transmitter. The data transmitted could be seen in the logic analyzer.

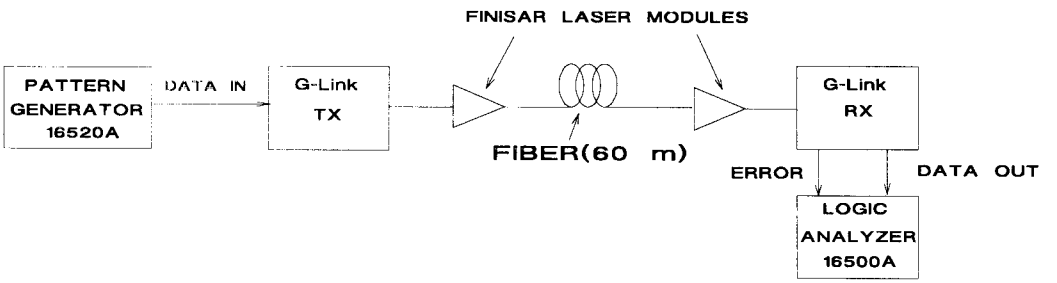

Figure 9: Pattern generator test setup

The tests above show that the implementation is possible but, they don't give much information about the data integrity during the transmission (Bit error rate). In order to provide that a dedicated hardware to test the bit error rate is been developed.

The high speed link described in this document and the low speed link (Ref.9) were implemented in a single print circuit board to provide communication between the Port Card and the SAR module .

6.Conclusion

The design issues of the high speed optical link was explained in detail. A low cost, high performance was proposed in accord to the application requirements.

7.References

1. Matulik. M et al, "D0 Silicon Vertex Detector System Interconnect Description", 1993.

2. Goff D., "High-Speed Data Transmission Over Multimode Fiber".

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7."Application Note - Digital Link Controller FCC-2000", Finisar Corporation.

8. "AT & T Multifiber Optical Cable Assemblies Product Catalog ", AT& T Microelectronics, September, 1993.