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2017 JINST 12 C03053

(http://iopscience.iop.org/1748-0221/12/03/C03053)

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Published by IOP Publishing for Sissa Medialab

Received: *November 16, 2016*
Revised: *January 26, 2017*
Accepted: *February 16, 2017*
Published: *March 13, 2017*

Topical Workshop on Electronics for Particle Physics,
26–30 September 2016,
Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany

LHCb Scintillating Fiber detector front end electronics design and quality assurance

W.E.W. Vink,[a,1] **A. Pellegrino,**[a,b] **G.C.M. Ietswaard,**[a] **J.C. Verkooijen,**[a] **U. Carneiro**[c] **and A. Massefferi**[c] **on behalf of LHCb SciFi collaboration**

[a] *Nikhef, National institute for subatomic physics, Amsterdam, The Netherlands*
[b] *University of Groningen, Groningen, The Netherlands*
[c] *CBPF Brazillian Center for Research in Physics, Rio de Janeiro, Brasil*

E-mail: wilco.vink@nikhef.nl

Abstract: The on-detector electronics of the LHCb Scintillating Fiber Detector consists of multiple PCBs assembled in a unit called Read Out Box, capable of reading out 2048 channels with an output rate of 70 Gbps. There are three types of boards: PACIFIC, Clusterization and Master Board. The Pacific Boards host PACIFIC ASICs, with pre-amplifier and comparator stages producing two bits of data per channel. A cluster-finding algorithm is then run in an FPGA on the Clusterization Board. The Master Board distributes fast and slow control, and power. We describe the design, production and test of prototype PCBs.

Keywords: Front-end electronics for detector readout; Manufacturing

[1] Corresponding author.

doi:10.1088/1748-0221/12/03/C03053

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1 Introduction

The LHCb detector will be upgraded during the Long Shutdown 2 (LS2) of the LHC in order to cope with higher instantaneous luminosities. Moreover, in order to increase the overall trigger efficiency, a 40 MHz readout scheme will be adopted in the on-detector electronics. The current tracking detectors downstream of the LHCb dipole magnet will be replaced by a Scintillating Fibre (SciFi) Tracker [1].

The Front-End (FE) electronics interfaces to the Silicon Photo Multipliers (SiPMs) on one side and to the experiment data-acquisition and control system on the other. It will consist of more than 4600 boards with more than 524,000 readout channels. In all the steps of design, validation and mass production, special care has to be taken to ensure that all boards are thoroughly tested. This article focuses on the strategy chosen to achieve this result, emphasizing the role of "*early design involvement*" of PCB manufacturers and assembly companies. First a general description of the SciFi electronics is given in section 2. Then a detailed description of the procedures put in place already during the design stage to ensure its manufacturability and testability is presented in section 3. Finally in section 4 an end-item test device is described, capable of performing the final validation of an entire readout unit with a series of functional tests.

2 Scintillating fiber detector front end electronics

The FE electronics interfaces to the SiPMs on one side and to the experiment data-acquisition and control system on the other. All SiPM signals are amplified, shaped and digitized in the 64-channel PACIFIC [2] ASIC; four PACIFIC ASICs are located on each PACIFIC Board. In order to reduce the data volume, the digitized channel data is routed to a flash-based IGLOO2 FPGA running a cluster-finding algorithm. Each Clusterization Board hosts two such FPGAs, processing the data

of 256 PACIFIC channels. The cluster data is then further sent to GBTX serializers located on the Master boards; four Clusterization Boards are connected to one Master Board. A Read Out Box (ROB) contains two Master Boards, eight Clusterization Boards, and eight PACIFIC Boards, and can service an entire SciFi module (2048 SiPM channels). The inter-connections between the three types of boards are realized through FMC connectors. The data serialized by the GBTX ASICs on the Master Board are shipped over optical fibers. An Housekeeping FPGA on the Master Board drives a Light Injection System (LIS) injecting light at the end of each fiber mat to provide SiPM gain calibration. The Master Board hosts 11 FeastMP DC-DC converters [3], providing four different voltages to the various devices in the ROB. Each ROB consumes about 110 W, and is individually cooled by demineralized water lines at 19°C.

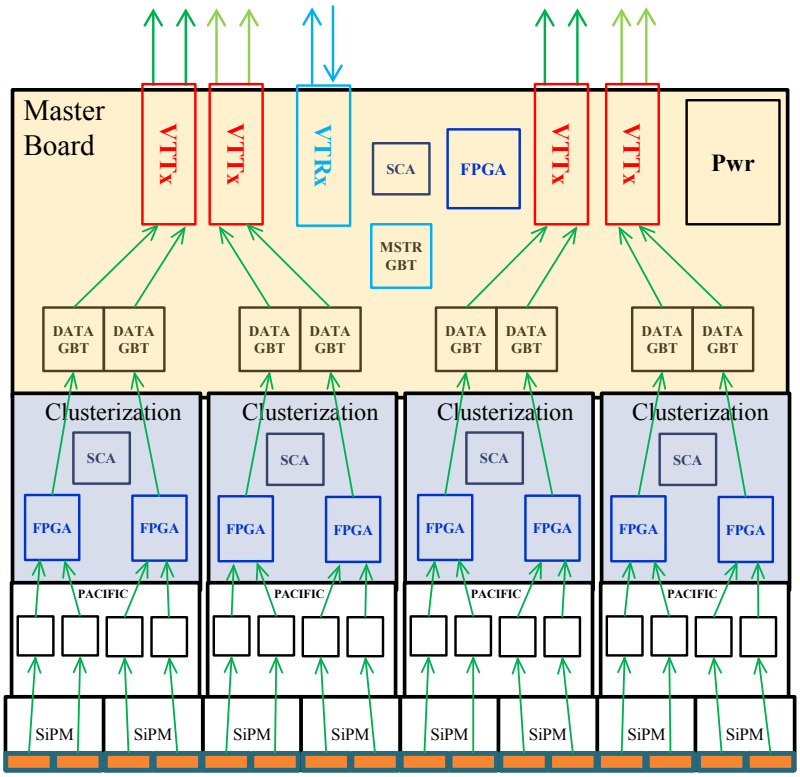

Figure 1. Block Diagram of half a ROB. The main components on each board are shown. The data flow is denoted by the green line.

The FE architecture is such that the cluster data of each SiPM are sent over a single fiber to the Back-End (BE) Electronics. Each ROB has also a complete interface for the distribution of bias voltages to the integrated circuits and to the SiPMs, of Timing and Fast Control (TFC) signals and of signals from and to the Experiment Control System (ECS). The communication with the TFC/ECS system goes via the GBT serial protocol: each Master Board hosts one Master GBT with an optical link connected to the LHCb SOL40 [6] detector control system. The entire clock tree is derived by deskewable clocks provided by the GBT. The clocks and fast-control commands are distributed to the Clusterization FPGAs and to the PACIFIC ASICs. For the slow control, five GBT-SCA ASICs [9] per half-ROB are used. The configuration of all devices is performed through

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SCA I^2C ports. The monitoring of the temperatures and of the SiPM bias voltages is based on the ADCs implemented in the SCAs. The SCA JTAG master is used to re-program all FPGAs.

All components are selected on the base of their radiation tolerance. The digitization of the SiPM signals is done by the 64-channel PACIFIC ASICs [2], the clustering algorithm is implemented in Microsemi M2GL090 FPGAs, and the data and control transmission uses the GBT chipset [4]. The power network implemented on the Master Board uses FeastMP DC/DC converters [3].

The LHCb SciFi detector consists of three tracking stations, each in turn consisting of four layers of scintillating-fibers modules. The active elements of a module are "mats" of scintillating material obtained stacking up six layers of round scintillating fibers with a diameter of 250 µm. Each module consists of 8 fiber mats. At one end of each fiber mat an 128-channel SiPM array is mounted [5]. Figure 2 shows a front view of the SciFi modules. The ROBs are attached at both ends of the modules. Each ROB consists of two boxes: a "Cold-Box" hosting 16 SiPM arrays (cooled down to −40°C) and a "FE-Box" containing the on-detector electronics previously described. The two are interconnected by flex cables. The SciFi on-detector electronics will consist of 256 ROBs, corresponding to 512 Master, 2048 Clusterization and 2048 PACIFIC Boards, for a total of about 524,000 readout channels.

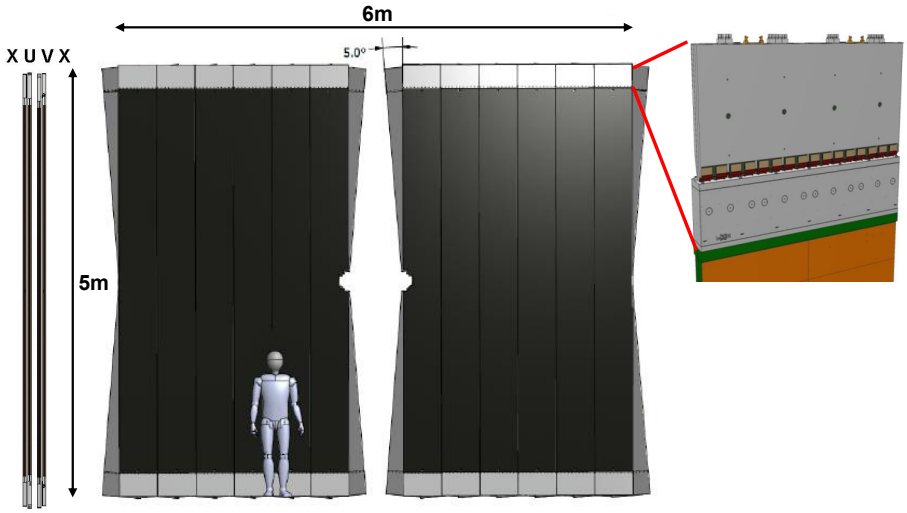

Figure 2. Overview of the SciFi fiber modules and Readout Boxes.

We produced and commissioned two ROB prototypes, including mechanical enclosure, cooling and shielding. We could successfully configure all devices on the ROB via the GBT serial links on the Master Board, using SOL40 firmware implemented on a prototype back-end electronics consisting of a MiniDAQ system based on the AMC40 architecture [7, 8]. In addition, we successfully demonstrated data transmission through the ROB, and could ship cluster data to the AMC40 MiniDAQ. We adopted the GBT "widebus" serial protocol at 4.48 Gbps, and a first implementation of the LHCb Tell40 DAQ framework in the AMC40, that processes incoming GBT data and produces 10GbE packets. We were able to perform a complete system test and demonstrated that the design of the SciFi FE architecture is ready to pass to the production phase.

An exploded-view drawing of a ROB is shown in figure 3, together with a picture of a half-ROB prototype. Clearly recognizable are the fiber-module end, the Cold-Box hosting the SiPMs, the flex

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cables connecting the SiPMs to the FE electronics, the various FE boards (Master, Clusterization and PACIFIC), and the metallic FE box providing cooling, grounding and shielding.

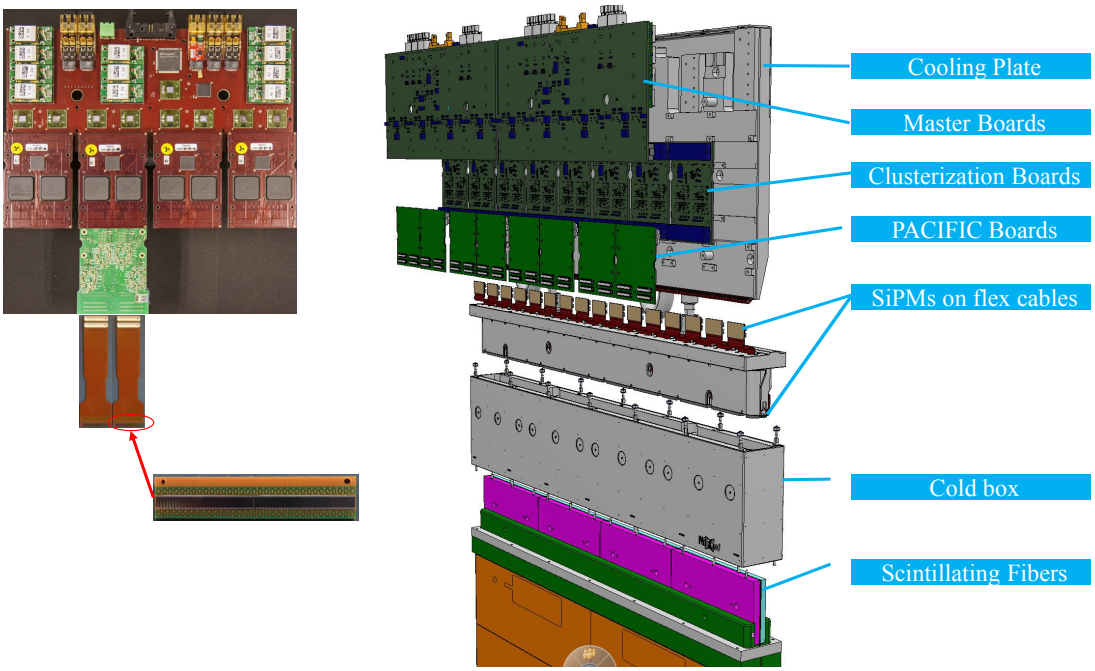

Figure 3. Image of the prototypes PCBs on the left and an exploded view of the Read Out Box including module, end piece, coldbox and electronics on a cooling frame.

As part of the prototype validation several cooling tests were performed. Figure 4 shows two infrared images of half a ROB; the temperature measured by three NTC sensors attached to some hot components are also shown. In the left panel one can see the temperature distribution without water flow in the right panel the temperature distribution with a water flow of 2 l/min.

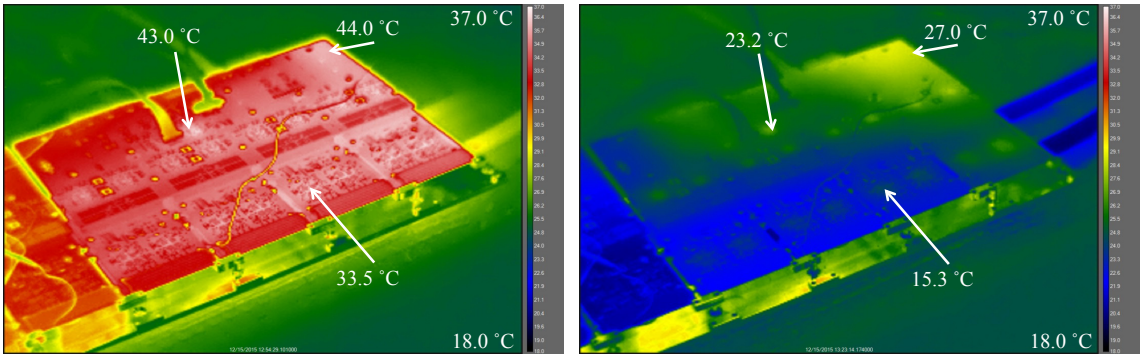

Figure 4. Thermal images taken during cooling test. Left panel: no water cooling. Right panel water flow of 2 l/min.

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3 Quality control of the PCB manufacturing

With 512 Master Boards, 2048 Clusterization Boards and 2048 PACIFIC Boards, to be produced and tested, a strategy to test all the boards, discard the faulty ones and ensure a satisfactory yield, need to be an integral part of the overall design process from the very beginning. The large number of components and nets on the PCBs make the design particulary complicated and error-prone. To give an example, nine 400 pins 0.8 mm pitch BGAs and a high number of *0402* capacitors and resistors are assembled on a single board. Moreover, all boards are expected to have a lifetime of ten to fifteen years in the LHCb detector.

While ECAD tools give the designer virtually unlimited design possibilities, the production processes at PCB manufacturer and assembly companies put several limitations of which the designer is not always aware, resulting in end items with a low production yield and limited lifetime. Therefore, the strategy chosen to meet these challenges emphasizes the role of "*early design involvement*" of PCB manufacturers and assembly companies. More specifically, for the design of the first prototypes of the Master and Clusterization boards we chose to implement two "Design For Excellence" (DfX) procedures [10]. A DfX typically consists of three phases during which design data is exchanged between the designer and the reviewer to guide the design during schematic entry, stack-up and layout, the first phase taking place before the design in the ECAD software starts, and the last phase taking place after the generation of production data. During each phase, the reviewer produces detailed reports describing the issues and giving design recommendations. The essential point is that the application of these DfX procedures guarantees that the production process will provide a given yield, quantified in terms of "slip through", i.e. the percentage of errors that could occur (mainly determined by those parts of the design that could not be made "testable").

Given the important role played in the SciFi electronics design process by the DfX procedures, and also considering that such procedures are rather uncommon in the design of electronics for particle and astro-particle physics experiments, they will be illustrated in more detail in the following sections. In particular, two DfX procedures will be considered separately: a "Design For Manufacturing" (DfM) one [11], to optimize the board design for the manufacturing and assembly process, and a "Design For Test" (DfT) one [12], to monitor the quality of the assembly process during and after the assembly of the boards. These two DfX procedures, DfM and DfT, are closely related and are applied in parallel during the design.

3.1 Design for Manufacturability

The main goal of the DfM process is to aid the design leading to a board that can be produced with the desired lifetime and yield. Figure 5 shows the three stages in which data is exchanged between the designer and the reviewer. Phase 0 is prior to the ECAD design: the reviewer delivers a set of design rules and the preferred data format for data exchange; the designer provides the reviewer with design specifications, block diagram(s) and the list of components. PCB materials (material properties, stack-up and trace width and clearances) and components suitable for lifetime and manufacturability are selected. After phase 0 the schematic entry starts and component footprints are created. Parts are placed on the preferred locations. The two outer copper layers are generated. In what is known as phase 1, schematics, outer copper layers with footprints and Bill Of Materials (BOM) are then

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reviewed. Footprints recommended by the component manufacturer are not always ideal for the assembly process. In some cases they need to be adapted to the assembly process. A trade off has to be established between components reliability and assembly process. The component placement determines the numbers of assembly stages; minimizing these can decrease the production cost. As an example: through-hole components are traditionally soldered by hand or by a (selective) wave soldering process; using Pin-In-Paste (PIP) components soldered during the reflow process supersedes the wave soldering process (larger pads become then necessary to hold the solder paste). The last phase can have several iterations, during which changes implemented by the designer as a result of the reviewer recommendations are checked. Once the complete layout is finished, a final check is done by the reviewer and a makeability report is before the manufacturing process starts.

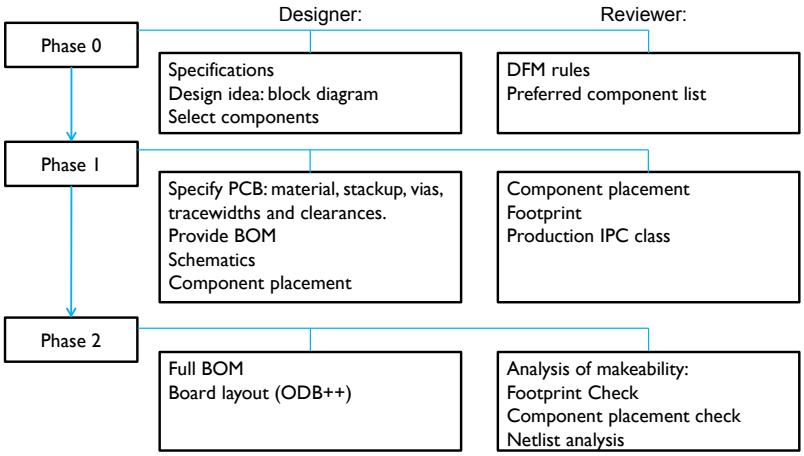

Figure 5. DfM process flow.

3.2 Design for Test

The DfT process aims at optimizing the design for testability. Its process flow is shown in figure 6. DfM and DfT run in parallel, and they share common data exchanged between the designer and the reviewer. The reviewer provides reports with the list of the tests that can provide the best test coverage at the lowest cost. In the last phase, a test strategy is chosen and the corresponding test coverage is reported. Several iterations of phase 2 are possible, to increase the coverage or decrease the cost. Typical tests that can be performed during or after production are:

- 3D Optical Automated inspection (3D-OAI). An optical PCB inspection will be done at three stages: the first one after applying the paste to check (against a pre-defined profile) whether the paste is correctly applied; the second one after the components are placed on the paste, eventually correcting erroneous placements of the parts; the third one after the reflow process to check the solder joints. 3D-OAI renders time-consuming and error-prone manual inspections superfluous.

- Automated X-ray Inspection (AXI). The solder joints of BGA parts are checked by X-ray inspection.

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- Flying Probe test (FPT). After the assembly, passive components, nets, and solder connections are tested with flying probes. To render this effective, as many testpoints as possible have to be foreseen to avoid using component pads, thus reducing the risk of damaging solder contacts.
- In Circuit Test (ICT). This is comparable to the FPT, but uses a custom-made needle card. It requires that all nets be accessible from the test side. Its main advantage with respect to the FPT is the shorter time needed.
- Extended Boundary Scan Test (EBST). All connections between boundary-scan capable devices are checked. Via passive and/or active loop-back board(s), connectors can be checked for defect solder contacts and broken nets.

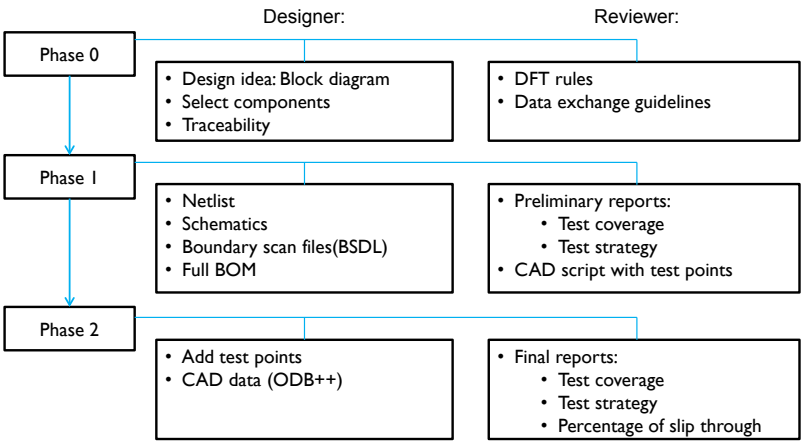

Figure 6. DfT process flow.

3.3 DfX results

Adopting DfM and DfT procedures in the SciFi prototype boards design resulted in boards that were free of production errors and could directly be used in functional tests without any need of electrical tests. The reviewer reports advised the test strategy shown in figure 7, with the expected coverage of each test (BGA X-ray inspection is a default test and therefore is not explicitly mentioned). The higher yield of the Clusterization board can be explained by its excellent boundary-scan coverage. The conclusion (small overall slip-through) is that if these procedures are followed for mass production, no dedicated electrical test of individual boards is required, and all boards can be directly assembled into a complete ROB, ready for the end-item test described in next section.

4 End-item FE Tester

End-item quality assurance of a complete FE Box requires a dedicated test setup capable of running a series of functional tests. An automatic FE Tester has been designed, consisting of a mechanical frame supporting several boards connected to the FE Box under test by flex cables. A schematic block diagram of the FE Tester is shown in figure 8. Control and data acquisition is performed with

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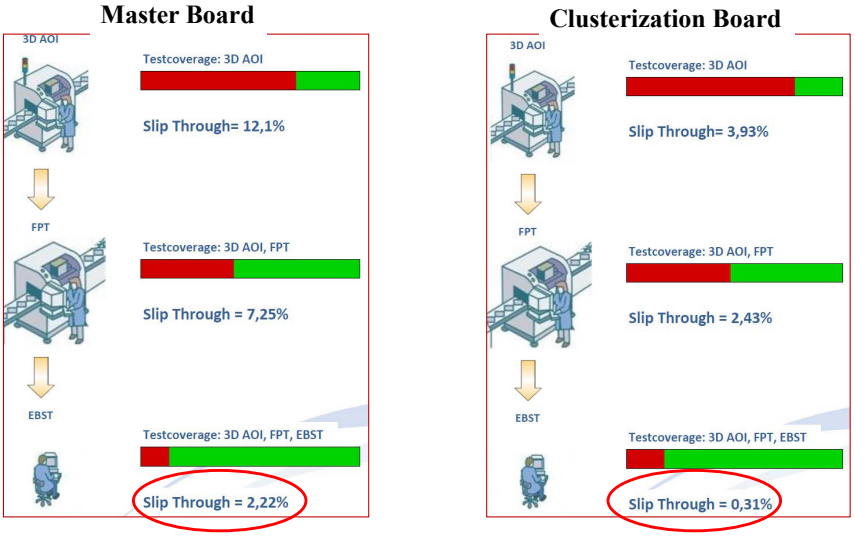

Figure 7. Advised test strategy and production slip through.

a MiniDAQ system, a generic system designed for the LHCb experiment. The FE Tester emulates the SiPM output pulses by a circuitry for each of the 2048 channels of a FE Box; due to the high density of components, this pulsed injector system consists of eight identical boards, each hosting a control FPGA. A control board hosting a GBT is the link between the MiniDAQ and the injector boards. A set of functional tests (channel-to-channel crosstalk, timing scans, threshold scans, etc.) will automatically be run controlled by procedures written in the standard LHCb WinCC SCADA software. All sixteen 4.8 Gb/s data optical links of the FE Box under test are read out by the MiniDAQ, and data are transferred to the host computer via 10 GbE and stored on disk, where data analysis jobs will produce a complete diagnosis, and store the results in a quality-assurance database. Beside aiding the quality assurance during mass production, the FE Tester will also be an indispensable diagnosis tool for the long-term mantainance and repair.

5 Conclusions

The LHCb detector will be upgraded during the Long Shutdown 2 (LS2) of the LHC in order to cope with higher instantaneous luminosities. The tracking detectors downstream of the LHCb dipole magnet will be replaced by the SciFi Tracker. The SciFi FE electronics will consist of more than 4600 boards with more than 524,000 readout channels. A complete strategy for the quality assurance of this electronics has been presented, consisting of several steps. In particular, the role of early-design involvement of the PCB manufacturing and assembly companies has been emphasized, and detailed Design-for-Manufacturing and Design-for-Test procedures, adopted already during the design stage, have been illustrated. The impact of these procedures on the first SciFi board prototypes have been presented, to show that boards free of production errors can be obtained. Quality control procedures have been identified that will allow mass production of Master boards and Clusterization Boards with yields of 97.78% and 99.69%, respectively. These high yields imply that the boards received from the producer(s) will not require additional tests before being

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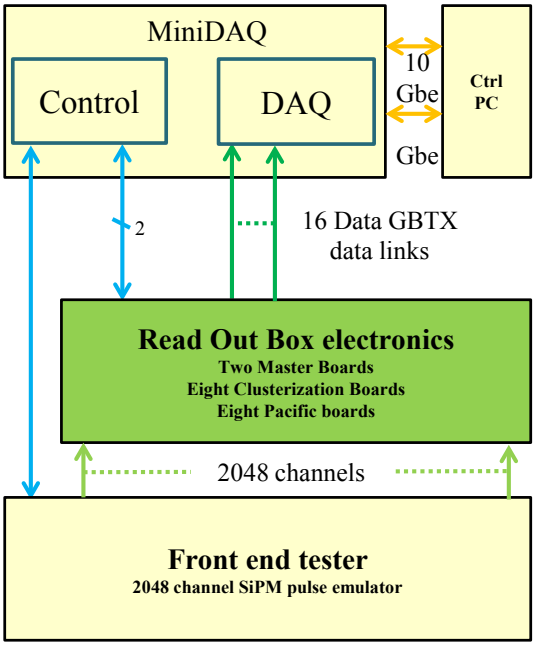

Figure 8. Block diagram of the SciFi full functional tester testing the ROB under test.

assembled into a complete FE Box. The quality assurance of each FE Box will be completed by an end-item test performed by a dedicated test setup, capable of running a series of functional tests that fully characterize the FE box, and of storing the results in a quality-assurance database for tracing.

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