



Multiple synchronous states in static delay-free mutually connected PLL networks

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ABSTRACT

In many engineering applications, the time coordination of geographically separated events is of fundamental importance, as in digital telecommunications and integrated digital circuits. Mutually connected (MC) networks are very good candidates for some new types of application, such as wireless sensor networks. This paper presents a study on the behavior of MC networks of digital phase-locked loops (DPLLs). Analytical results are derived showing that, even for static networks without delays, different synchronous states may exist for the network. An upper bound for the number of such states is also presented. Numerical simulations are used to show the following results: (i) the synchronization precision in MC DPLLs networks; (ii) the existence of synchronous states for the network does not guarantee its achievement and (iii) different synchronous states may be achieved for different initial conditions. These results are important in the neural computation context, as in this case, each synchronous state may be associated to a different analog memory information.

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1. Introduction

Since the 1970s, an important issue in the implementation of many engineering systems is the distribution of synchronous clock signals in a network of geographically separated nodes. Systems designed for this specific purpose are called phase tracking or synchronization networks [1]. Synchronization networks are part of the core of digital telecommunication networks [2]; power generation systems [3]; integrated digital circuits [4] and sensor networks [5].

The Master Slave (MS) technique has become dominant in clock distribution engineering in the last decades due to its easy implementation and management and because MS networks are able to present good results for the synchronization problem, specially for the case of

digital telecommunications [6–8]. However, recently, new applications, for which Mutually Connected (MC) implementations seem a more natural solution, are developing fast. The main examples are the time signal distribution in digital electronic circuits [9–11] and sensor networks [12–16].

MC networks of oscillators may also be used to implement neural computational systems. In this context, a network is said to be synchronized if all nodes oscillate with the same frequency, leading to constant phase-differences between them. If different vectors of phase-differences can be achieved, each one can be associated to a memory information [17]. Neuro-computers can be implemented by using MC networks with dynamic connectivity between nodes [18], so that different synchronous states may be achieved depending on the connection pattern [17,19,20] and on the local parameters of the nodes [21].

In this work, a network of MC digital phase-locked loops (DPLLs) is considered [22–24] and it is shown that in a DPLL network with saw-tooth phase-detectors, there

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may be multiple synchronous states even for static delay-free networks.

In [11], the existence of these states is discussed and a technique to change the stability of the non-desired ones is presented. In fact, in classical applications of synchronization networks, the existence of multiple stable synchronous states for a network must be avoided. However, when neural computation is considered [18], multiple stable synchronous states are desired and the higher the number of such states, the higher the memory capacity.

The major contribution here is to show that, for a network of non-identical nodes, the number of synchronous states in this type of network may grow very fast with network size. We present lower and upper bounds for the number of such states and confirm with numerical experiments, that a single network can reach different synchronous states, depending only on the initial phase differences between nodes. We believe this is a promising architecture for the implementation of neuro-computers because information could be stored in an analog form, following the concept proposed in [25].

Section 2 presents a brief description of the network model developed in [18,26]. Section 3 brings analytical results derived for synchronous states of the network, showing the existence of multiple synchronous state for a network. Section 4 presents three numerical results: (i) time intervals between transitions tend to be equal when synchronous state is achieved in a noise-free network; when noise is considered, the synchronization precision is the same as the oscillators precision; (ii) the existence of a synchronous state in the network does not guarantee its achievement; and (iii) when considering fixed values for all network parameters, depending on the initial conditions of the network, multiple synchronous states may be achieved. Section 5 summarizes possible future applications.

2. The DPLL network model

In this section, a brief description of DPLL network model is presented, in order to provide a basis and to establish the notation.

2.1. The single DPLL model

All phase-locked loops (PLL) implementations can be modeled as a closed-loop composed of a phase detector (PD), a low-pass filter (LPF), and a voltage controlled oscillator (VCO) [22–24].

In DPLLs, the input signal, $v_i(t)$, and the VCO output, $v_o(t)$, are digital with levels 0 and V_{dd} . Calling this type of PLLs *digital PLLs* may be controversial [23] and here, the nomenclature used in [22] is followed, although the term DPLL can also be reserved for circuits in which all signals are digital, as in [24].

Fig. 1 shows a block diagram of the model to be used here. The VCO generates square waves with frequency depending on the input voltage v_c according to:

$$\dot{\Theta} = f + \delta f \left(\frac{v_c}{V_{dd}} - \frac{1}{2} \right), \quad (1)$$

where f is the VCO central frequency and δf its loop gain. More accurate models for real devices may be implemented by using look-up tables to consider the nonlinear behavior of VCOs [27]; however, for the purposes of this work, the linear model suffices.

PDs are implemented with JK flip-flops, with one of its inputs inverted [22]. The output signal of the VCO is inverted before comparison. In this way, the PD operation can be described by a simple rule: positive transitions in the reference signal, v_i , produce positive transitions in the output, v_d ; and negative transitions in the internal signal of the PLL, v_o , produce negative transitions in v_d .

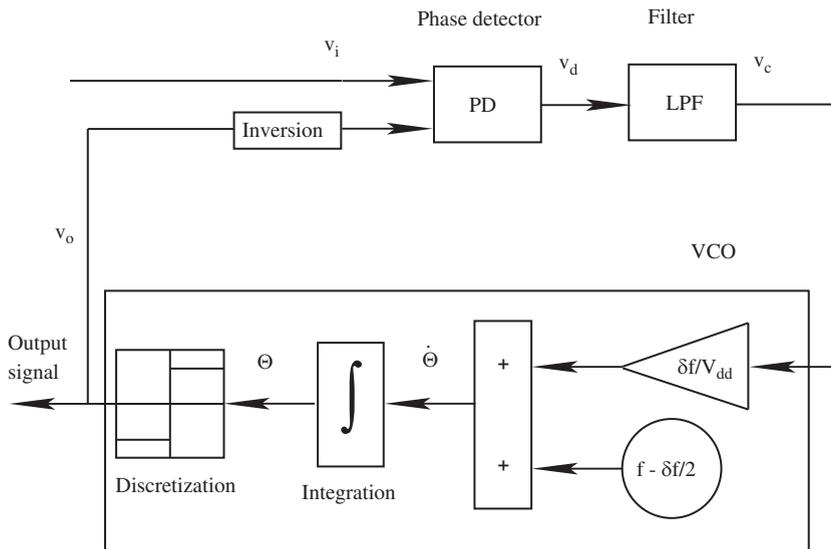


Fig. 1. Block diagram of a single DPLL.

The filter is considered to be stable linear first order low-pass [28], with transfer function $F(s)$, avoiding bifurcations and chaotic attractors [29] as used in the main commercial integrated PLL [22].

The LPF transfer function given by:

$$F(s) = \frac{f_c}{s + f_c}, \tag{2}$$

with f_c being the cut-off frequency Hz.

2.2. Network model

Considering a n node network, node i , with a block diagram shown in Fig. 2, receives signals from the other $n-1$ nodes of the network. As all phase comparisons must be independent, each network node is composed of $n-1$ PDs, $n-1$ filters, and one VCO. This model is a generalization of the one proposed in [30], which can be obtained by identically setting all the node filters.

PD_{ji} is the node i phase detector, which compares its internal signal, v_o^i , with the input signal coming from node j , v_j^i . The output of PD_{ji} is denoted v_d^{ji} . In the same way, LPF_{ji} is the low pass filter from node i , the input signal of which is v_d^{ji} , and v_p^{ji} is its output signal. The cut-off frequency of filter LPF_{ji} is denoted by f_c^{ji} .

The coupling matrix $\mathbf{C} = (c_{ji})_{n \times n}$ of the network is defined so that the VCO input of node i is given by:

$$v_c^i = \sum_{j=1}^n c_{ji} v_p^{ji}. \tag{3}$$

As $0 \leq v_p^{ji} \leq V_{dd}$, matrix \mathbf{C} must have the property that $\sum_{j=1}^n c_{ji} = 1; \forall i$, which assures that $0 \leq v_c^i \leq V_{dd}, \forall i$.

The VCO model of the i -th node of the network is obtained from equations (1) and (3):

$$\dot{\theta}^i = f_i + \delta f_i \left(\frac{\sum_{j=1}^n c_{ji} v_p^{ji}}{V_{dd}} - \frac{1}{2} \right), \tag{4}$$

where f_i and δf_i are the central frequency and the loop gain of node i , respectively.

Considering a reference frequency f_0 , corresponding to a period $T_0 = 1/f_0$, a non-dimensional variable $\hat{t} = t/T_0 = f_0 t$ is used as an independent variable to measure time and to take derivatives. Defining $W_i = f_i/f_0$ as the normalized central frequency of node i , $\delta W_i = \delta f_i/f_0$ as the normalized loop gain of node i , and $F_c^{ji} = f_c^{ji}/f_0$ as the normalized filter cut-off frequency, the normalized model for the VCO of node i can be written as

$$\dot{\theta}^i = W_i + \delta W_i \left(\frac{\sum_{j=1}^n c_{ji} v_p^{ji}}{V_{dd}} - \frac{1}{2} \right). \tag{5}$$

3. Existence of synchronous states for the network

In this section, some analytical results about the synchronous state of the network are derived.

First, phase detector PD_{ji} is considered. According to the description of the PD behavior given in Section 2.1, the phase detector output, v_d^{ji} , will have a positive transition whenever the input from node j , v_j^i has a positive transition; and a negative transition whenever the internal signal of node i , v_o^i , has a negative transition. Consequently, the PD output will have a duty cycle equal to 0.5 if signals v_j^i and v_o^i are in phase, i.e., $\Delta\theta_{ji} = \theta^j - \theta^i = 0$. If $\Delta\theta_{ji}$ is positive, the duty cycle value increases to 1.0, when $\Delta\theta_{ji} = 0.5$. If $\Delta\theta_{ji}$ is negative, the duty cycle decreases to 0.0, when $\Delta\theta_{ji} = -0.5$. Therefore, the PD_{ji} output has a duty cycle given by $DC_{ji} = \Delta\theta_{ji} + 0.5$, for $-0.5 \leq \Delta\theta_{ji} \leq 0.5$.

An usual assumption in the study of these systems is that, in synchronized states, the phase differences are small, making the previous equation a model for the phase detector operation [11,31–33]. Here, however, this is not assumed and, since the nonlinear behavior of the PD is taken into account, a corrected phase difference, Ξ , needs to be defined as

$$\Xi_{ji} = \Delta\theta_{ji} - \text{floor}(\Delta\theta_{ji} + 0.5), \tag{6}$$

with $\text{floor}(x)$ being the greatest integer which does not exceed the real number x . Therefore, the duty-cycle, DC , of the PD output is given by:

$$DC_{ji} = \Xi_{ji} + 0.5. \tag{7}$$

Considering Eq. (7), it is possible to predict the filter mean output value as a function of the phase differences of the signals, in the long term. In this way, considering a network with n nodes, the filter output LPF_{ji} can be written as a function of phase difference Ξ_{ji} as

$$v_p^{ji} = DC \cdot V_{dd} = (\Xi_{ji} + 0.5)V_{dd}. \tag{8}$$

It is important to notice that, under these conditions, filter dynamics can be neglected, as the model is developed to obtain results about the network synchronous state, only.

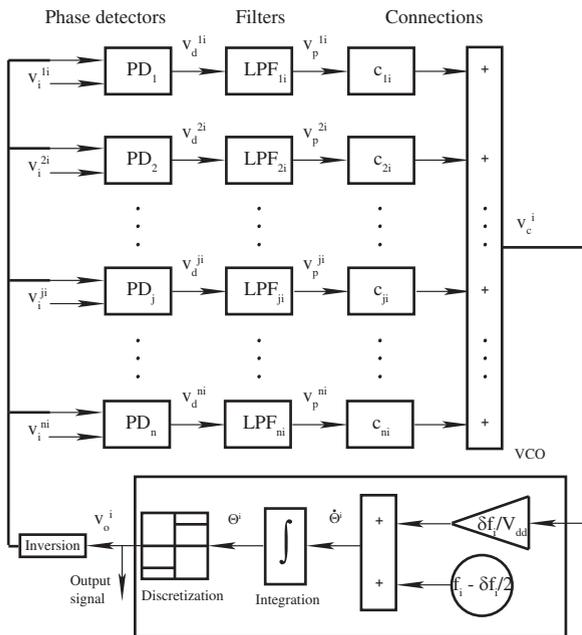


Fig. 2. Block diagram of a DPLL assembled in MC network.

Replacing Eq. (8) in (5) and considering that $\sum_{j=1}^n c_{ji} = 1$:

$$\dot{\theta}^i = W_i + \delta W_i \left(\sum_{j=1}^n c_{ji} \varepsilon_{ji} \right). \quad (9)$$

3.1. Synchronous state of the network

In the synchronous state, all nodes of the network oscillate with the same frequency, that is: $\dot{\theta}^1 = \dot{\theta}^2 = \dots = \dot{\theta}^n = W_s$.

With the model given by Eq. (9), the synchronous state of the network is given by the following system of equations:

$$W_s = \dot{\theta}^i = W_i + \delta W_i \left(\sum_{j=1}^n c_{ji} \varepsilon_{ji} \right), \quad i = 1 \dots n. \quad (10)$$

Considering that $-0.5 \leq \varepsilon_{ji} \leq 0.5$, the value of ε_{ji} can be obtained from the values of ε_{j1} and ε_{i1} by:

$$\varepsilon_{ji} = \varepsilon_{j1} - \varepsilon_{i1} + \alpha_{ji}, \quad i, j = 1 \dots n, \quad (11)$$

with:

$$\alpha_{ji} = \begin{cases} 0 & \text{if } |\varepsilon_{j1} - \varepsilon_{i1}| \leq 0,5; \\ +1 & \text{if } \varepsilon_{j1} - \varepsilon_{i1} < -0,5; \\ -1 & \text{if } \varepsilon_{j1} - \varepsilon_{i1} > 0,5. \end{cases} \quad (12)$$

This definition makes possible to conclude that $\alpha_{ii} = 0$, $\alpha_{i1} = 0$ and $\alpha_{ji} = -\alpha_{ij}$.

Consequently, Eq. (10) may be written as functions of the phase differences between all nodes and node 1. Performing algebraic manipulations, this system of equations is given by:

$$Ax^T = B, \quad (13)$$

with

$$A = \begin{bmatrix} 1/\delta W_1 & -c_{21} & \dots & -c_{j1} & \dots & -c_{n1} \\ 1/\delta W_2 & 1 & \dots & -c_{j2} & \dots & -c_{n2} \\ \vdots & \vdots & \ddots & \vdots & \ddots & \vdots \\ 1/\delta W_i & -c_{2i} & \dots & 1 & \dots & -c_{ni} \\ \vdots & \vdots & \ddots & \vdots & \ddots & \vdots \\ 1/\delta W_n & -c_{2n} & \dots & -c_{in} & \dots & 1 \end{bmatrix}, \quad (14)$$

$$x = [W_s \ \varepsilon_{21} \dots \varepsilon_{i1} \dots \varepsilon_{n1}], \quad (15)$$

and

$$B = \begin{bmatrix} \frac{W_1}{\delta W_1} \\ \frac{W_2}{\delta W_2} + \sum_{j=1}^n \alpha_{j2} c_{j2} \\ \vdots \\ \frac{W_i}{\delta W_i} + \sum_{j=1}^n \alpha_{ji} c_{ji} \\ \vdots \\ \frac{W_n}{\delta W_n} + \sum_{j=1}^n \alpha_{jn} c_{jn} \end{bmatrix}. \quad (16)$$

The solution of system (13) completely determines the synchronous state of the network.

However, it is important to consider that: (i) system (13) must be solved for all the combinations of α ; (ii) for every solution, it is necessary to verify the agreement between α s and the phase differences obtained as solution.

Additionally, it can be noticed that, although the total number of α s is n^2 , the number of independent values is reduced to $N_\alpha = (n^2 - 3n + 2)/2$ because $\alpha_{ji} = -\alpha_{ij}$, $\alpha_{ii} = 0$ and $\alpha_{i1} = 0$. Therefore, the only coefficients α_{ji} that should be verified are with indexes given by $i = 2 \dots n$ and $j = i + 1 \dots n$.

Another restriction about these N_α coefficients can be exemplified with a 4-node network, where $N_\alpha = 3$; more specifically, α_{32} , α_{42} and α_{43} . If, for instance, $\alpha_{32} = 1$, it implies $\varepsilon_{31} < 0$. Therefore, $\alpha_{43} \neq 1$, thus $\alpha_{32}\alpha_{43} \neq 1$. With similar arguments, it is possible to show that $\alpha_{43}\alpha_{42} \neq -1$ and $\alpha_{42}\alpha_{32} \neq -1$.

The total number of different sets of coefficients α for the 4-node network would be given by $N_s = 3^{N_\alpha} = 3^3 = 27$; however, when considering these restrictions, this number is reduced to $N_s = 13$, an upper bound for the number of possible synchronous states for a 4-node network.

In the general case, all these restrictions can be written in the form:

$$\begin{aligned} \alpha_{jk}\alpha_{ji} &\neq -1; \\ \alpha_{pi}\alpha_{ji} &\neq -1; \\ \alpha_{pj}\alpha_{ji} &\neq 1. \end{aligned} \quad (17)$$

A last important consideration for system (13) is: regardless of the coefficients set chosen, the system synchronous state frequency, if the symmetry condition $c_{ij} = c_{ji}$ holds, is always given by:

$$W_s = \frac{\sum_{i=1}^n \frac{W_i}{\delta W_i}}{\sum_{i=1}^n \frac{1}{\delta W_i}}, \quad (18)$$

which is obtained by the sum of all the equations of system (13).

This result is exactly the same as the one obtained in [15], where a general odd nonlinear phase detector characteristic is considered. This was expected because our PD characteristic is also odd. However, it is also demonstrated in [15], with the additional assumption that the PD characteristic is an increasing and continuously differentiable function, that if a synchronous state for the network exists, the synchronous state is globally asymptotically stable.

As in the case analyzed here, the PD characteristic does not satisfy these conditions, global stability of the synchronous state cannot be guaranteed. It will be shown later that, in fact, the existence of a synchronous state for the network does not guarantee that it will be achieved for all initial conditions. In the same way as for analog (LPLLs) [34], the reachability of existing synchronous states depends on the filters cut-off frequencies, nodes loop gains and initial phase differences between nodes.

3.2. A synchronization criterion

In this section, it will be considered that $\delta W_i = \delta W$ for $i = 1 \dots n$, so that Eq. (18) becomes:

$$W_s = \frac{\sum_{i=1}^n W_i}{n}, \quad (19)$$

that is, if the loop gain of all nodes is the same, the synchronous state frequency of the network is given by the mean value of the central frequencies of the network nodes.

Another assumption is that, for all $i \neq j$, $c_{ji} = 1/(n-1)$, and $c_{ii} = 0$. With both assumptions, Eq. (9) for two nodes u and v may be written as

$$\begin{aligned} \varepsilon_{1u} + \varepsilon_{2u} + \dots + \varepsilon_{nu} &= \frac{(n-1)(W_s - W_u)}{\delta W} \\ \varepsilon_{1v} + \varepsilon_{2v} + \dots + \varepsilon_{nv} &= \frac{(n-1)(W_s - W_v)}{\delta W}. \end{aligned} \quad (20)$$

Subtracting the above equations:

$$(\varepsilon_{1u} - \varepsilon_{1v}) + (\varepsilon_{2u} - \varepsilon_{2v}) + \dots + (\varepsilon_{nu} - \varepsilon_{nv}) = \frac{(n-1)(W_v - W_u)}{\delta W}. \quad (21)$$

We choose $\alpha_{ji} = 0, \forall i, j$; thus $\varepsilon_{vu} = \varepsilon_{v1} - \varepsilon_{u1}$, since the purpose in this section is to determine a choice of δW that guarantees the existence of at least one possible synchronous state for the network. Consequently, Eq. (21) can be written as

$$\varepsilon_{vu} = \frac{(n-1)(W_u - W_v)}{n\delta W}. \quad (22)$$

To guarantee the coherence of the phase differences of the synchronous state with the choice of coefficients, α it is only necessary to guarantee that $|\varepsilon_{vu}| < 0.5 \forall u, v$. This condition can be stated as

$$\delta W_L > \frac{2(n-1)}{n} (W_{max} - W_{min}), \quad (23)$$

where W_{max} and W_{min} the maximum and minimum central frequencies of the network nodes, respectively.

Consequently, one may conclude that, for $\delta W \geq \delta W_L$, there is at least one synchronous state for the network.

These results are related only with the existence of synchronous states for the network. The achievement of these states is not guaranteed from any initial condition, differently from the case of continuous PD characteristic [15,35].

4. Numerical results

Considering the DPLL network model from Section 2 and the analytical results derived, this section shows some numerical experiments for the dynamical behavior of the network. For all simulations, the filters were integrated considering a bilinear transformation and the VCO dynamics was evaluated with a simple Euler method. In addition, a linear interpolation algorithm was used to determine the VCO output transition times, as in [36]. The integration step of 0.001 was used for all cases.

4.1. Synchronization precision

To verify the transient behavior of the network, a 4-node network with central frequencies $W_1 = 0.85$, $W_2 = 0.95$, $W_3 = 1.05$ and $W_4 = 1.15$ was mounted. The coupling weights were set to $c_{ji} = 1/3$, if $i \neq j$, and $c_{ii} = 0$. The cut-off frequencies of the filters were set to 1.

Considering the criteria given by Eq. (23), if $\delta W > 0.45$, there is at least one possible synchronous state for the network. Choosing $\delta W = 0.6$ for all nodes and solving system (13) for all combinations of coefficients α_{32} , α_{42} and α_{43} , there is only one possible synchronous state given by $W_s = 1$, $\varepsilon_{21} = 0.125$, $\varepsilon_{31} = 0.25$ and $\varepsilon_{41} = 0.375$.

Fig. 3 shows the values of ε_{21} , ε_{31} and ε_{41} obtained by numerical simulation. If the initial phases of all nodes are set to 0, the results present no qualitative difference related to that obtained when other values are used.

From Fig. 3, it is possible to see that the simulation results are in accordance with the analytical ones. However, even in synchronous state, phase differences present oscillations. To verify the importance of these oscillations to the synchronization quality, in Fig. 4(a) the time intervals between VCO positive transitions for all nodes are plotted.

As one can see from Fig. 4(a), the oscillations of the phase differences do not cause oscillations in the time interval between transitions. To verify the synchronization quality, simulations were conducted for a total time of $\hat{t} = 100$, varying the integration step. For each simulation, the standard deviation of the time interval between transitions for all nodes was calculated for the interval $50 < \hat{t} < 100$, so that the long term behavior of the system was already achieved. Fig. 5 shows the values of these standard deviations as a function of the integration step.

Fig. 5 shows a relation between the integration step used in simulations and the standard deviation observed for the periods of the nodes. This result indicates that, although phase differences between nodes oscillate, the time interval between transitions for all nodes tends to be equal. Simulations were conducted for different network parameters with results confirming this hypothesis.

Another verification about the quality of synchronization considers noisy VCOs for the nodes. Only phase noise characterized by the standard deviation d of the time interval between positive transitions in the VCO output was considered. We set the value of d to 10^{-4} for all nodes. The resulting standard deviation of time intervals between transitions for different integration steps are also shown in Fig. 5. It is possible to verify that for noisy VCOs, for integration steps smaller than 10^{-4} , the standard deviation for the time intervals between transitions stays at 10^{-4} . As expected, using VCOs with 10^{-4} precision leads to a synchronization of the network with errors of the order of 10^{-4} .

4.2. Non-achievable synchronous states

Section 3.2 proposed a synchronization criterion that guarantees the existence of at least one synchronous state for a given distribution of central frequencies for the

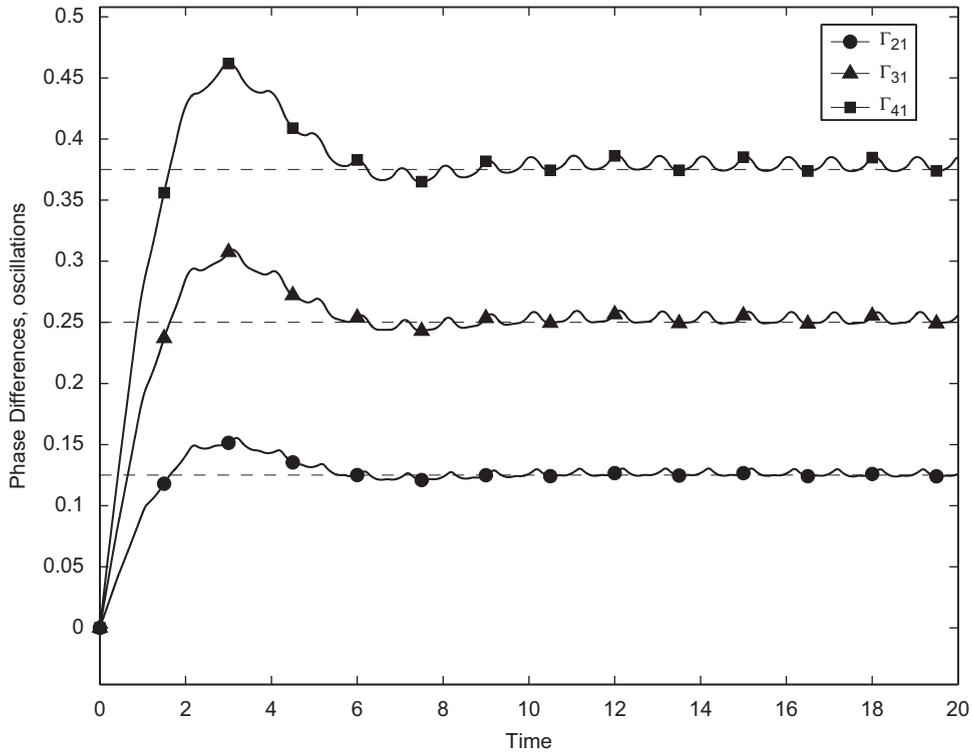


Fig. 3. Phase differences between nodes for a 4-node network with $W_1 = 0.85$, $W_2 = 0.95$, $W_3 = 1.05$ and $W_4 = 1.15$. The values $\mathcal{E}_{21} = 0.125$, $\mathcal{E}_{31} = 0.25$ and $\mathcal{E}_{41} = 0.375$ obtained by analytical methods for the synchronous state are indicated in dotted lines.

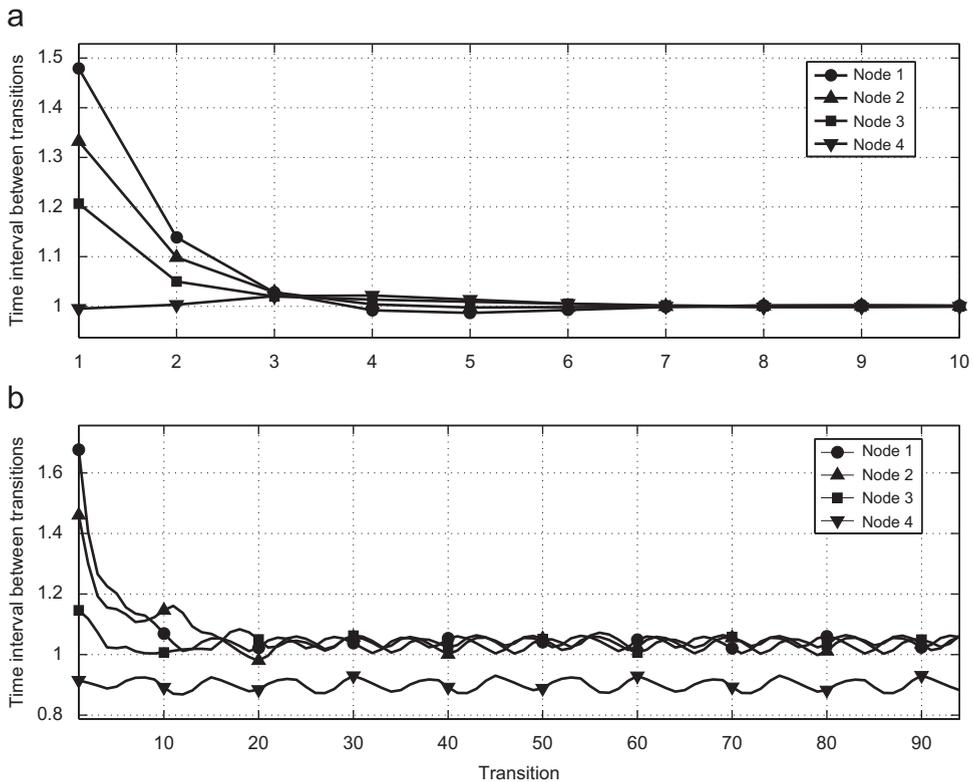


Fig. 4. Time intervals between VCO positive transitions for the 4-node network with $W_1 = 0.85$, $W_2 = 0.95$, $W_3 = 1.05$ and $W_4 = 1.15$. The loop gain of all nodes are set to $\delta W = 0.6$. (a) The cut-off frequencies of all filters are set to $F_c = 1$. (b) The cut-off frequencies of all filters are set to $F_c = 0.25$.

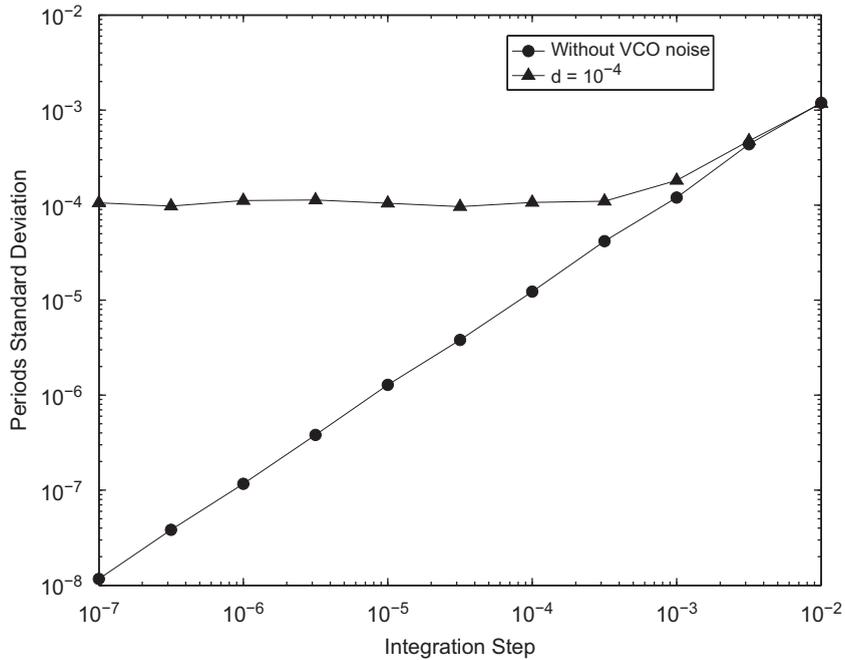


Fig. 5. Standard deviations of the time intervals between transitions for different integration steps. For both cases, the network parameters are $W_1 = 0.85$, $W_2 = 0.95$, $W_3 = 1.05$ and $W_4 = 1.15$, $F_c = 1$ and $\delta W = 0.6$. Simulations were conducted for a total time $\hat{t} = 100$ and the standard deviations were calculated for $50 < \hat{t} < 100$. Results are indicated for the case of noise-free oscillators and for the network having oscillators with precision $d = 10^{-4}$.

network. For the network considered in the previous section, where $W_1 = 0.85$, $W_2 = 0.95$, $W_3 = 1.05$ and $W_4 = 1.15$, Eq. (23) gives $\delta W > 0.45$. On the other hand, the synchronization criterion is based on the simplified behavior of the system, given by Eq. (9), which is not valid for the transient behavior. Therefore, it can be argued that the existence of a synchronous state does not guarantee that it will be achieved.

To verify this situation, the network considered in the previous section was simulated with different filter cut-off frequencies. It was changed from the previous 1.0 value to 0.25 and the time intervals between transitions are shown in Fig. 4(b). It can be concluded that, although the synchronous state for the network exists, for this choice of filter cut-off frequency, the synchronous state is not achieved.

In order to verify when the existing synchronous state is achieved as a function of the filter cut-off frequencies, simulations for the same distribution of central frequencies were conducted, changing δW and F_c , $F_c^{ij} = F_c \forall i, j$. The values of δW were set between 0 and 1.7, because the smallest central frequency is equal to 0.85. F_c varied between 0.01 and 2.

In both cases, the variation step was 0.01. For all simulations, the integration step was set to 0.001 and the total number of simulated periods was tuned according to the cut-off frequencies, in order to guarantee that the long term behavior of the system was achieved. The network is considered to be in a synchronous state if the time interval between the last simulated transition of all nodes is not more than one integration step different from the mean value of the time

interval between the last transitions of all nodes. Fig. 6 shows the results.

In Fig. 6, three separated regions are identified. The first, on the left of the figure, corresponds to points where there is no synchronous state. For these points, no synchronous state is achieved in the simulations. On the right side of the line corresponding to the synchronization criteria, there are two other regions so that there is at least one synchronous state. The network in which the time intervals between transitions are plotted in Fig. 4(a) is indicated in Fig. 6, as *simulation 1*, and it is an example of the case in which the synchronous state is achieved.

On the other hand, as in the case of the network in which the time interval between transitions are plotted in Fig. 4(b), it is possible to see that, for small values of δW and F_c , the synchronous state is not achieved, as shown in Fig. 6 as *simulation 2*.

To study why the existing synchronous state may not be achieved, Fig. 4(b) shows that for *simulation 2* the frequency of nodes 1, 2 and 3 gets closer to one another, which is not true for node 4. Furthermore, it can be noticed that for the network to synchronize, the phase difference between nodes 4 and 1 should be equal to $\Xi_{41} = 0.375$. In Fig. 7, the value Ξ_{41} is plotted for the cases of *simulation 1*, (a) and *simulation 2*, (b).

In Fig. 7(a), it is possible to see that the value of Ξ_{41} stops increasing after passing the threshold ($\Xi_{41} = 0.375$) before being greater than 0.5, when a slip occurs. In the case of Fig. 7(b), as the cut-off frequency of the filters is small ($F_c = 0.25$), the system is not fast enough and, consequently, the value of Ξ_{41} does not stop increasing before exceeding the limit of 0.5.

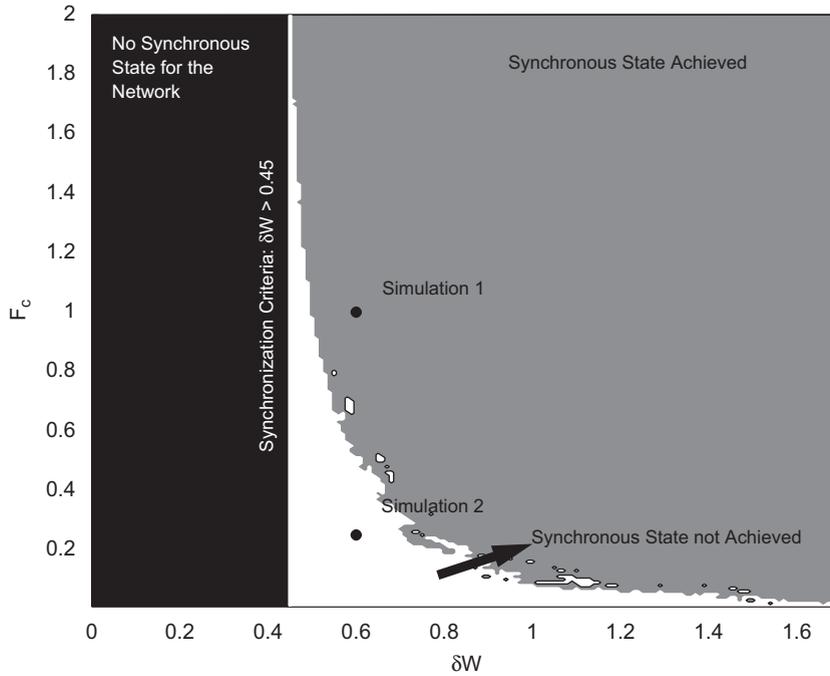


Fig. 6. Verification of whether or not a synchronous state is achieved for a 4-node network with $W_1 = 0.85$, $W_2 = 0.95$, $W_3 = 1.05$ and $W_4 = 1.15$. Each point in the figure corresponds to a simulation conducted for a different pair of parameters δW and F_c . δW changes between 0 and 1.7, while F_c varies between 0.01 and 2, both with step 0.01. The three regions correspond to configurations for which (i) no synchronous state exists; (ii) at least one synchronous state exists, but is not achieved and (iii) at least one synchronous state exists and is achieved.

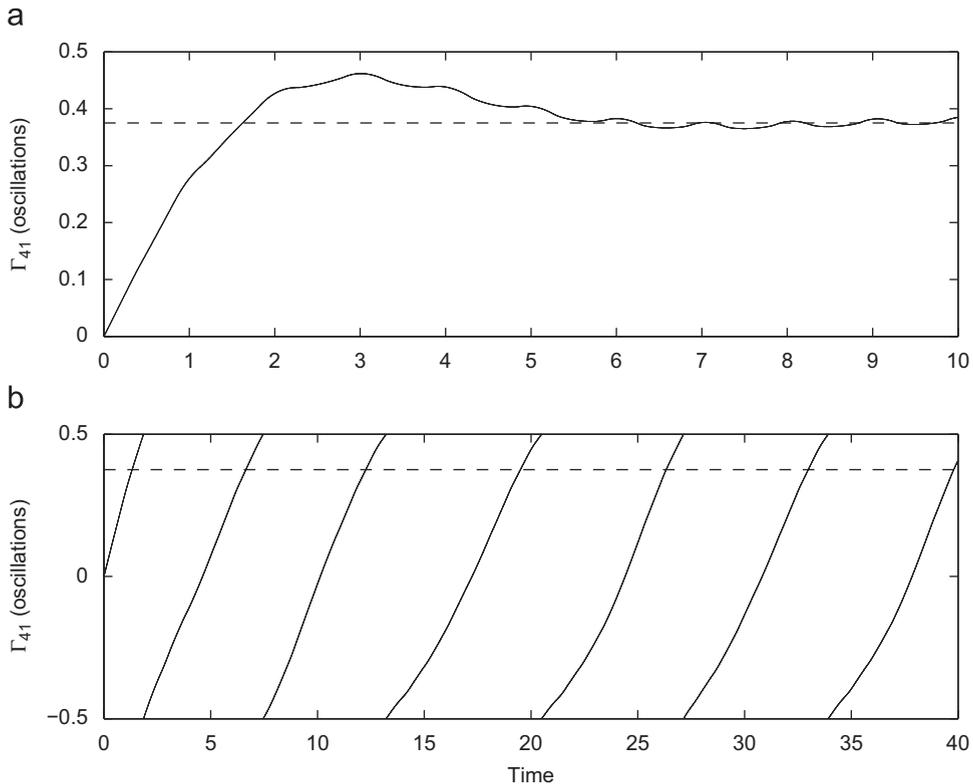


Fig. 7. $\bar{\varepsilon}_{41}$ is plotted as a function of time for the 4-node networks. The value $\bar{\varepsilon}_{41} = 0.375$ corresponding to the synchronous state is indicated in dotted lines. (a) $F_c = 1$. (b) $F_c = 0.25$.

In other words, the existing synchronous state may not be achieved because the system is too slow. Simulations were conducted considering the PD output to be given by Eq. (8), and the only difference observed is that the phase differences in synchronized states do not present oscillations; however, synchronization is achieved for exactly the same values of δW and F_c . From these results and the ones presented in [15], it is possible to conclude that synchronization may not be achieved, even if a synchronous state exists, due to the fact that the PD characteristic is not continuous, associated with the lag behavior associated with the presence of the filter.

4.3. Multiple synchronous states

As mentioned in Section 3.1, all possible synchronous states of a network of DPLLs can be determined by the solution of system (13). However, it was also noticed that, to find these states, one should solve the system for every possible parameter combination and verify the coherence between the choice of parameters and the results obtained. For a better understanding of the synchronous states that a DPLL network may achieve, a simple 3-node network is chosen as an example.

For a 3-node network, all connection weights c_{ji} are equal to 0.5, because of the symmetry assumption for the coupling matrix C and the condition $\sum_{j=1}^n c_{ji} = 1$, for all i . The node central frequencies are set to $W_1 = 0.97$, $W_2 = 1$ and $W_3 = 1.03$, the filter cut-off frequencies are set to 0.5 and the node loop gains are set to 0.5.

In this case, there is only one independent value of parameter α , α_{32} . Therefore, system (13) must be solved 3 times considering $\alpha_{32} = -1$, $\alpha_{32} = 0$ and $\alpha_{32} = 1$. For the

chosen parameters of the network, all the three systems lead to coherent synchronous states. For $\alpha_{32} = -1$, the phase differences obtained are $\Xi_{21} = -0.2933$ and $\Xi_{31} = 0.4133$ so that $|\Xi_{31} - \Xi_{21}| > 0.5$ corresponding to the value of α_{32} . For $\alpha_{32} = 0$ the solution is $\Xi_{21} = 0.04$ and $\Xi_{31} = 0.08$ and for $\alpha_{32} = 1$ the solution is $\Xi_{21} = 0.3733$ and $\Xi_{31} = -0.2533$.

So as to verify which the network synchronous state achieved was, numerical simulations were conducted for a total time $\hat{t} = 40$ and the value of the initial phase differences $\Xi_{21}(0)$ and $\Xi_{31}(0)$ were between -0.5 and 0.5 , with step 0.005. Fig. 8 shows the achieved synchronous state, corresponding to $\alpha_{32} = -1$, $\alpha_{32} = 0$ or $\alpha_{32} = 1$, depending on the initial phase differences.

So as to identify which the achieved synchronous state is, first the same method used in the preparation of Fig. 6 is applied to determine if frequency synchronization is achieved. Then, the phase-differences in the synchronous state are compared with the ones obtained by analytical methods allowing the determination of which the achieved synchronous state was. In the figure, the three synchronous states are represented by circles.

It is possible to observe that there is no preferential synchronous state. The fact that the one achieving more times corresponds to $\alpha = 0$ is explained because the size of the region in which $\Xi_{32} = \Xi_{31} - \Xi_{21} \pm 1$ is larger than the ones in which $\Xi_{32} = \Xi_{31} - \Xi_{21} \pm 1$.

For a more detailed analysis of the system behavior, Fig. 9(a) and (b) plot the phase differences Ξ_{21} and Ξ_{31} , as functions of time for two different initial conditions. For Fig. 9(a), the initial phase differences are given by $\Xi_{21}(0) = -0.2$ and $\Xi_{31}(0) = 0.2$, and the achieved synchronous state is the one corresponding to $\alpha_{32} = 0$. For the case of Fig. 9(b), $\Xi_{21}(0) = -0.4$ and $\Xi_{31}(0) = 0.2$

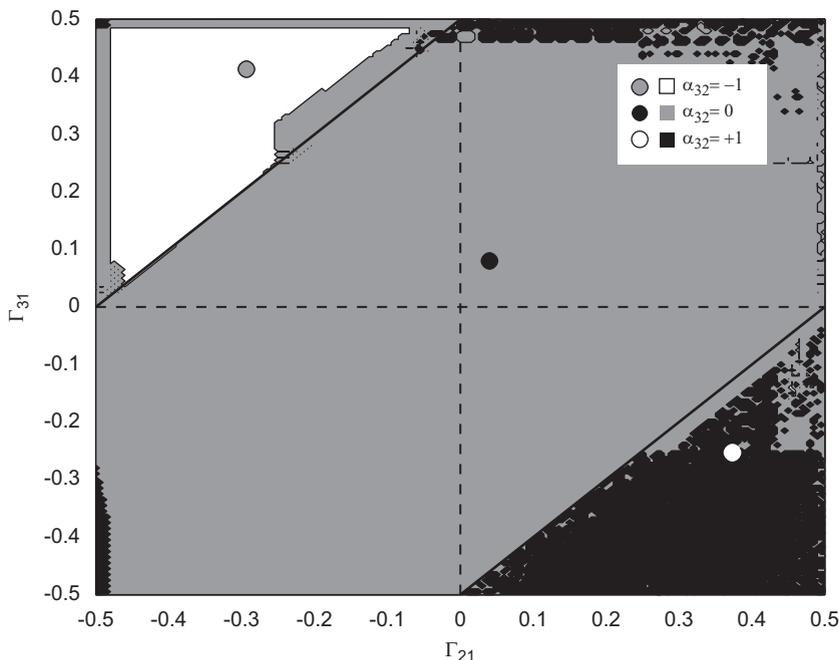


Fig. 8. Synchronous state achieved as a function of the initial phase differences for a 3-node network with $W_1 = 0.97$, $W_2 = 1$ and $W_3 = 1.03$.

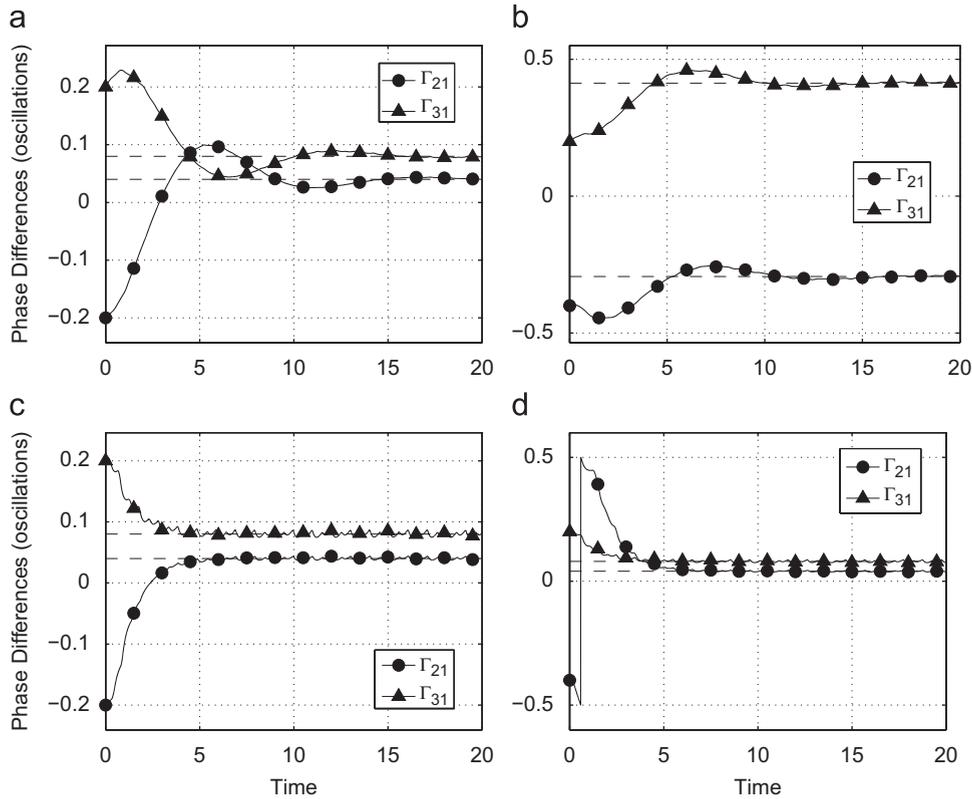


Fig. 9. Phase differences between nodes for different initial conditions and cut-off frequencies of the nodes. For all cases $W_1 = 0.97$, $W_2 = 1.0$ and $W_3 = 1.03$. For cases (a) and (b) the cut-off frequencies of the filters are set to 0.5, while for cases (c) and (d) they are set to 5. In cases (a) and (c) the initial phase differences are equal to $\Xi_{21}(0) = -0.2$ and $\Xi_{31}(0) = 0.2$, and in cases (b) and (d) the initial values are $\Xi_{21}(0) = -4.2$ and $\Xi_{31}(0) = 0.2$.

and the synchronous state achieved corresponds to $\alpha_{32} = -1$.

Another point of merit, considering the existence of multiple synchronous states for the system, is that the value of the cut-off frequencies of the filters can affect the synchronous state to be achieved. Considering the same initial phase differences as the ones used for Fig. 9(a) and (b), Fig. 9(c) and (d) show the phase differences for the same network with the cut-off frequencies of the filters being changed to 5. As can be observed, for cases (a) and (c) the change in the filter cut-off frequencies changes the transient behavior of the system, but the achieved synchronous state does not change. The same conclusion cannot be derived from the comparison of cases (b) and (d), when changes in the filters modify the achieved synchronous state.

5. Conclusions

The results presented in this work reinforce the hypothesis that considering linear coupling between nodes in MC networks of oscillators, although mathematically simple, avoids the identification of some important features of these systems, such as the multiple synchronous state existence.

These multiple synchronous states that appear even for static networks may be considered as an advantage

or a disadvantage, depending on the type of application. For the case of implementing of synchronization networks, it is a complicating factor, as the synchronous state of the network may change depending on the presence of errors during operation. On the other hand, when considering synchronous states as memory information in neural-computing devices, the multiplicity of these states may represent a marked increase in the computational capacity.

Future work may concern other types of network implementations: different types of couplings and other topologies such as nearest neighbor, random graphs and small-world networks may be good candidates to be studied when implemented with DPLL nodes. Another extension of this work is to study the topological properties of synchronization optimized networks following methods already implemented for other types of node dynamics [37,38]. Finally, if actual implementation of neuro-computers is to be considered, it is necessary to consider other complicating aspects of the node model, as, for example, VCO nonlinearity.

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